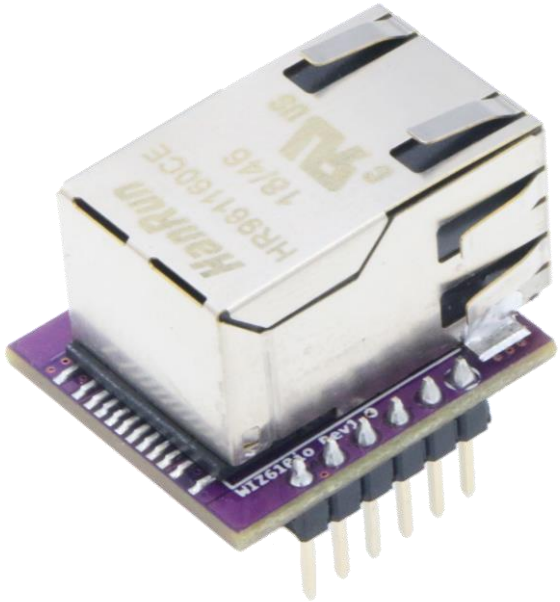
WIZ610io User Manual

(Version 1.1)



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Document Revision History

Date	Revision	Changes
2019-02-18	V1.0	Official Release
2019-05-30	V1.1	Verify modification, Add IO Module Carrier Board Description

1. Introduction

WIZ610io is the internet offload network module that includes W6100 (TCP/IP hardwired chip, include PHY), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W6100 and Transformer.

The WIZ610io is an ideal option for users who want to develop their Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W6100 Datasheet.

WIZ610io consists of W6100 and MAG-JACK.

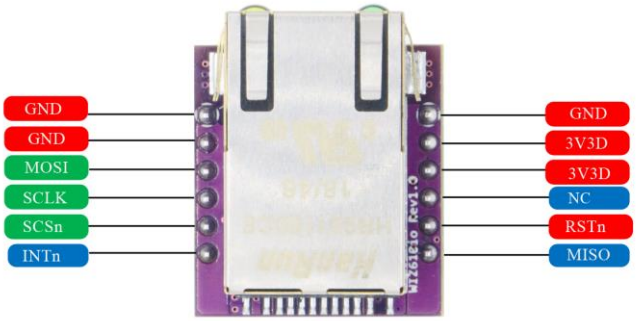
- Hardware TCP/IP, Ethernet MAC : Included in W6100
- Ethernet PHY : Included in W6100
- Connector : MAG-JACK(RJ45 with Transformer)

1.1 Feature

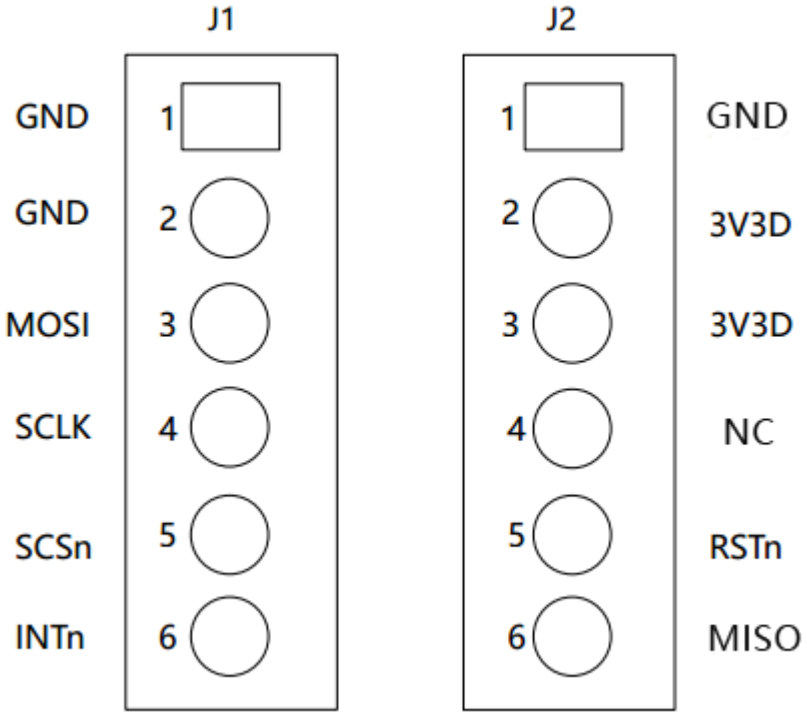
- Support Hardwired TCP/IP Protocols : TCP, UDP, IPv6, IPv4, ICMPv6, ICMPv4, IGMP, MLDv1, ARP, PPPoE
- Support IPv4/IPv6 Dual Stack
- Support 8 independent SOCKETs simultaneously with 32KB Memory
- Support SOCKET-less Command:
  ARP, PING, ICMPv6(PING, ARP,DAD,NA,RS) Command for IPv6 Auto-configuration& Network Monitoring
- Support Ethernet Power Down Mode & Main Clock Switching for power save
- Support Wake on LAN over UDP
- Support Serial Interface: High Speed SPI(MODE 0/3)
- Internal 16Kbytes Memory for TX/ RX Buffers
- 10BaseT/100BaseTX Ethernet PHY Integrated
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Support Auto-MDIX only on Auto-Negotiation Mode
- 3V operation with 5V I/O signal tolerance
- Network Indicator LEDs (Full/Half Duplex, Link, 10/100 Speed, Active)
- Interfaces with two 2.54mm pitch 1 x 10 header pin
- Temperature : -40 ~ 85℃(Operating)

2. Pin assignment & description

2.1 WIZ610io Pin assignment



< TOP side view >



< Pin assignment >

Pin Type Notation

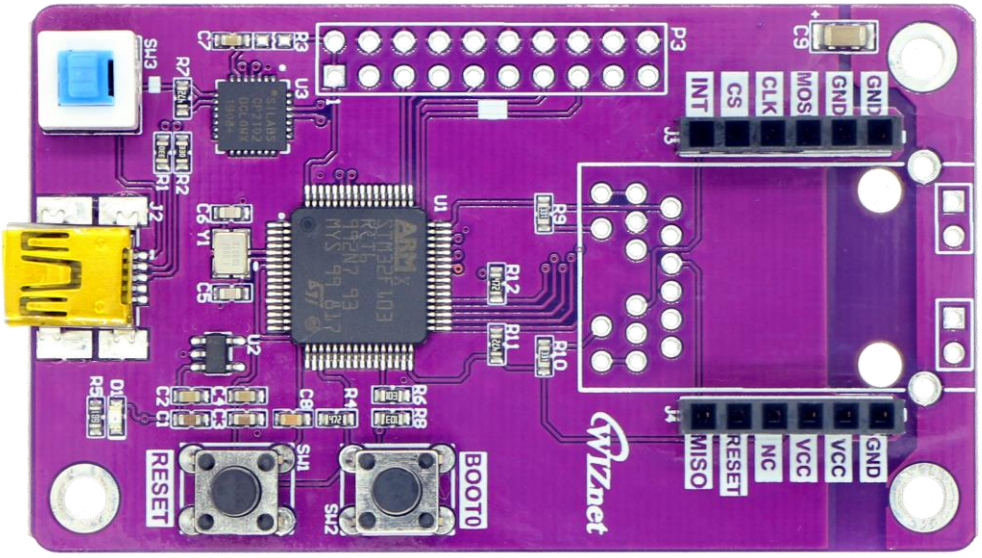
Type	Description
I	Input
O	Output
P	Power & Ground

2.1.2 WIZ610io Pin description

Pin No.		I/O	Pin Name	Description
J1	1	P	GND	**Ground**
	2	P	GND	**Ground**
	3	I	MOSI	**SPI Master Out Slave In** This pin is used to SPI MOSI signal pin.
	4	I	SCLK	**SPI Clock** This pin is used to SPI Clock Signal pin.
	5	I	SCSn	**SPI Slave Select :** Active Low This pin is used to SPI Slave Select signal Pin when using SPI interface.
	6	O	INTn	**Interrupt** : Active low When the event occur during W6100 Ethernet Communication, INTn notices to HOST. Low : Interrupt Occurred High : No Interrupt Refer to IEN (Interrupt pin Enable) in SYCR1 (System Config Register1), INTPTMR (Interrupt Pending Time Register), IR (Interrupt Register), SIR (Socket Interrupt Register), SLIR (SOCKET-less Interrupt Register).
J2	1	P	GND	**Ground**
	2	P	3V3D	**Power** : Digital 3.3V power
	3	P	3V3D	**Power** : Digital 3.3V power
	4	I	NC	**NC**
	5	I	RSTn	**Reset :** RSTn initializes W6100. RSTn must

				be asserted to Low longer than 1.0us. After asserted RSTn, W6100 spends 60.3ms for initialization. Low : W6100 initialized. High : Normal Operation.
	6	**O**	**MISO**	**SPI Master In Slave Out** This pin is used to SPI MISO signal pin.

2.2.1 IO Module Carrier Board



< TOP side view >

3. WIZ610io SPI operations

WIZ610io is controlled by a set of instruction that is sent from a external host , commonly referred to as the SPI Master. The SPI Master communicates with W6100 via the SPI bus, which is composed of four signal lines: Slave Chip Select (SCSn), Serial Clock (SCLK), MOSI (Master Out Slave In) and MISO (Master In Slave Out).

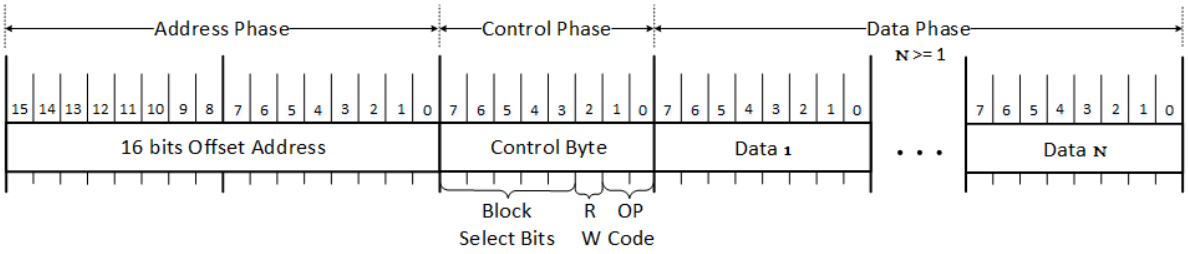
The SPI protocol defines four modes for its operation (Mode 0-3). Each mode differs according to the SCLK polarity and phase - how the polarity and phase

control the flow of data on the SPI bus. The W6100 operates as SPI Slave device and supports the most common modes - SPI Mode 0 and 3.

The only difference between SPI Mode 0 and 3 is the polarity of the SCLK signal at the inactive state. With SPI Mode 0 and 3, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

3.1 Process of using general SPI Master device

1. Configure Input/Output direction on SPI Master Device pins.
2. Configure SCSn as 'High' on inactive
3. Write target address for transmission on SPDR register (SPI Data Register).
4. Write Control Byte for transmission on SPDR register.
5. Write desired data for transmission on SPDR register.
6. Configure SCSn as 'Low' (data transfer start)
7. Wait for reception complete
8. If all data transmission ends, configure SCSn as 'High'



< W6100 SPI Frame Format >

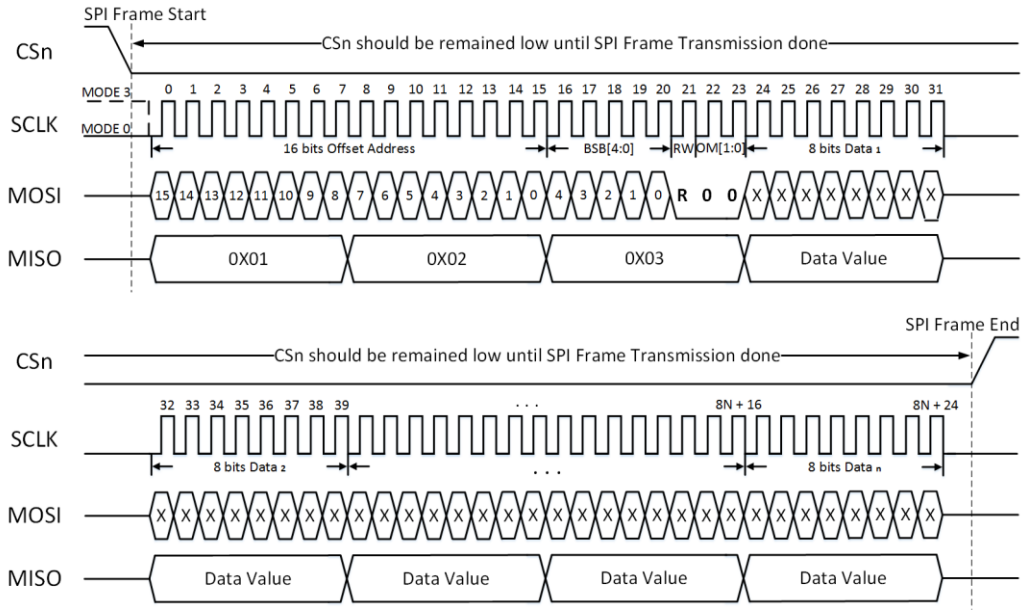
3.2 Read processing

In the VDM, CSn(High-to-Low) by HOST informs the start of SPI frame and CSn(Low to High) by HOST informs the end of SPI frame to W6100.

In the control phase, RW is "0" to indicate read access and OP[1:0] is "00" to indicate VDM.

The data bits received through MISO are synchronized to SCLK (Falling-Edge).

If more than one byte of data is transmitted continuously, it supports sequential data write.



< Read Sequence >

```
uint8_t tAD[3];   //send buffer
// Address
tAD[0] = (uint8_t)((AddrSel & 0x00FF0000) >> 16);
tAD[1] = (uint8_t)((AddrSel & 0x0000FF00) >> 8);
tAD[2] = (uint8_t)(AddrSel & 0x000000ff);

wizchip_cs_select(); //CS=0, SPI start

tAD[2] |= (_W6100_SPI_READ_ | _W6100_SPI_OP_);   // Control Byte

wizchip_spi_write_buf(tAD,3); //write address
for(idx = 0; idx < len; idx++)                    // Write data in loop
{
      buf[idx] = IINCHIP_SpiSendData(0x00);
 }
```

```
wizchip_cs_deselect();//CS=1, SPI end
```

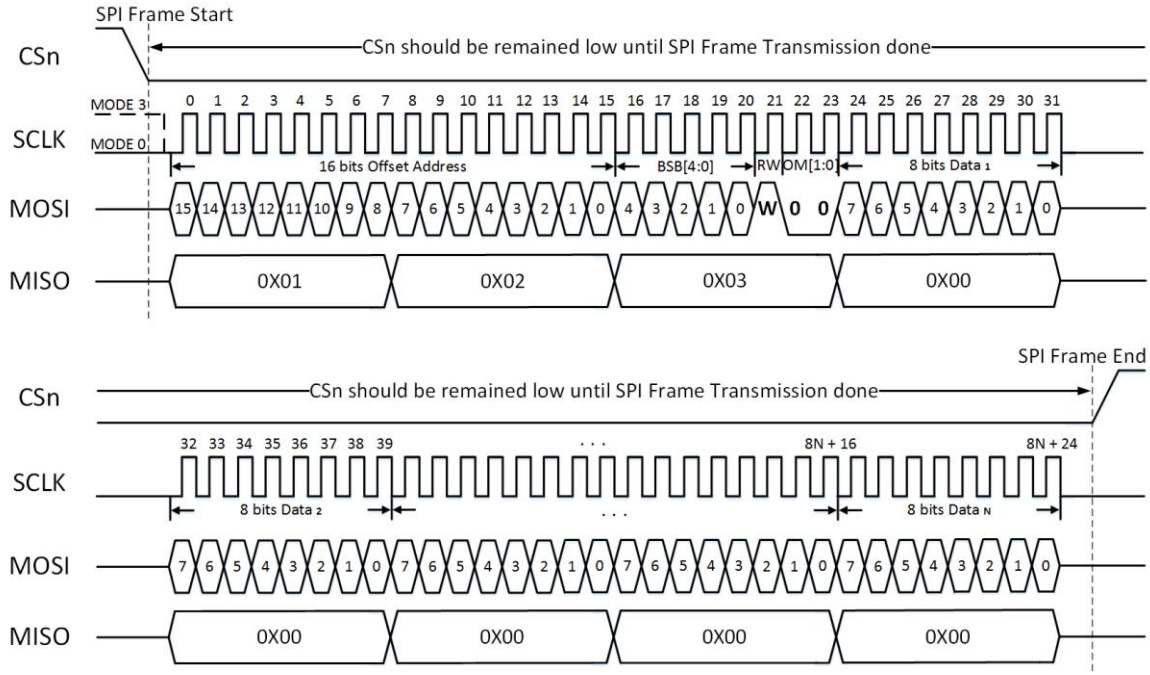
3.3 Write processing

In the VDM, CSn(High-to-Low) by HOST informs the start of SPI frame and CSn(Low to High) by HOST informs the end of SPI Frame to W6100.

In the control phase, RW is "1" to indicate write access and OM[1:0] is "00" to indicate VDM.

The data bits transmitted through MOSI are synchronized to the SCLK (Falling-Edge).

If more than one byte of data is transmitted continuously, it supports sequential data write.



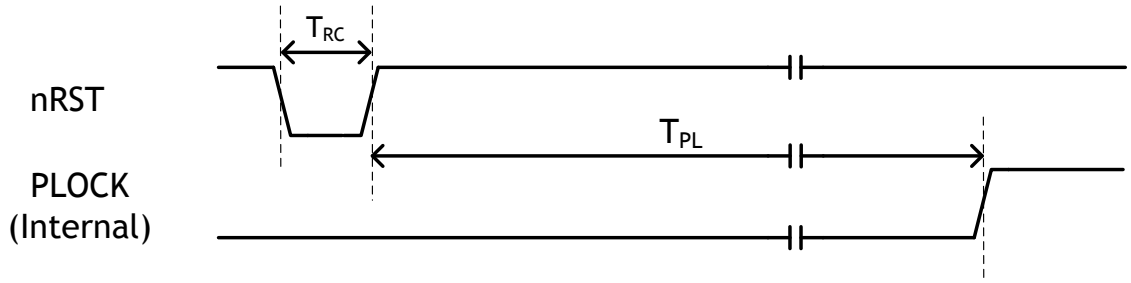
< Write Sequence >

```
uint8_t tAD[3];   //send buffer
 // Address
 tAD[0] = (uint8_t)((AddrSel & 0x00FF0000) >> 16);
 tAD[1] = (uint8_t)((AddrSel & 0x0000FF00) >> 8);
 tAD[2] = (uint8_t)(AddrSel & 0x000000ff);
 wizchip_cs_select(); //CS=0, SPI start

 tAD[2] |= (_W6100_SPI_WRITE_ | _W6100_SPI_OP_);   // Control Byte
```

```
    wizchip_spi_write_buf(tAD, 3);   //write data
    for(idx = 0; idx < len; idx++)                    // Write data in loop
    {
        IINCHIP_SpiSendData(buf[idx]);
    }

wizchip_cs_deselect();//CS=1, SPI end
```

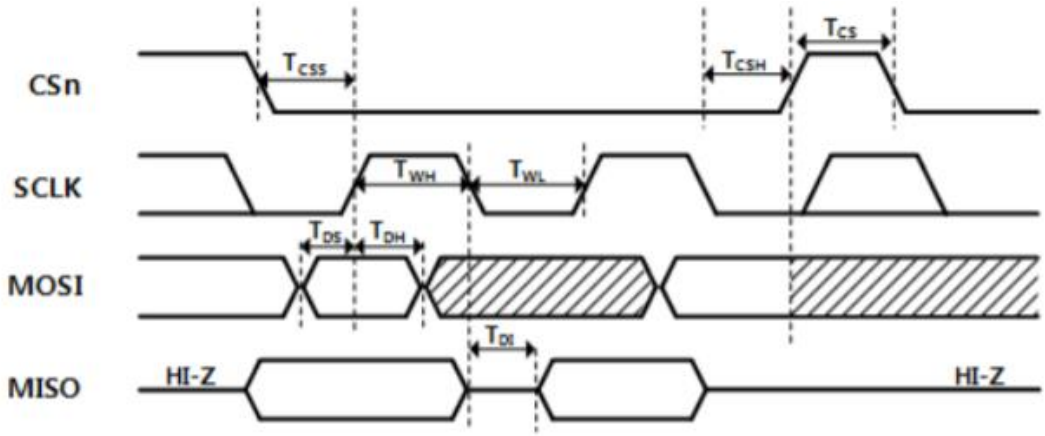
4. Timing diagram

4.1 Reset Timing



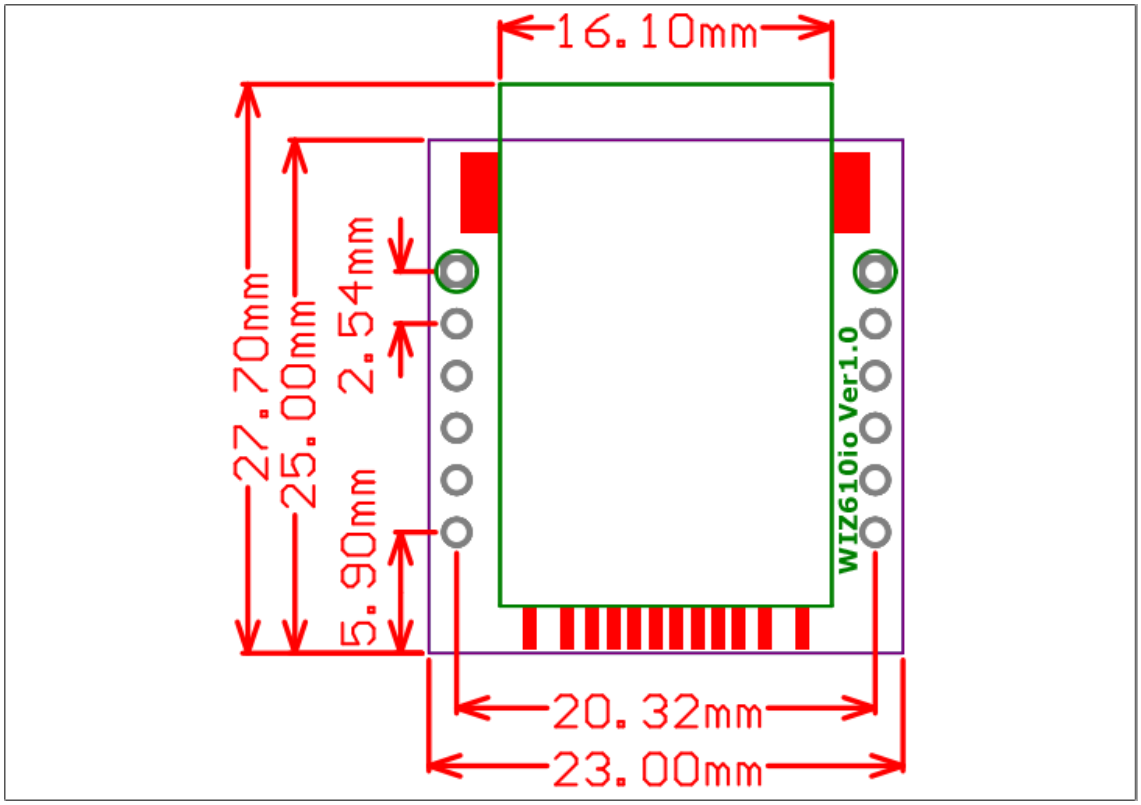
Symbol	Description	Min	Typ	Max
T_{RC}	Reset Time	350ns	580ns	1.0us
T_{PL}	Stable Time	-	-	60.3ms

4.2 SPI Timing



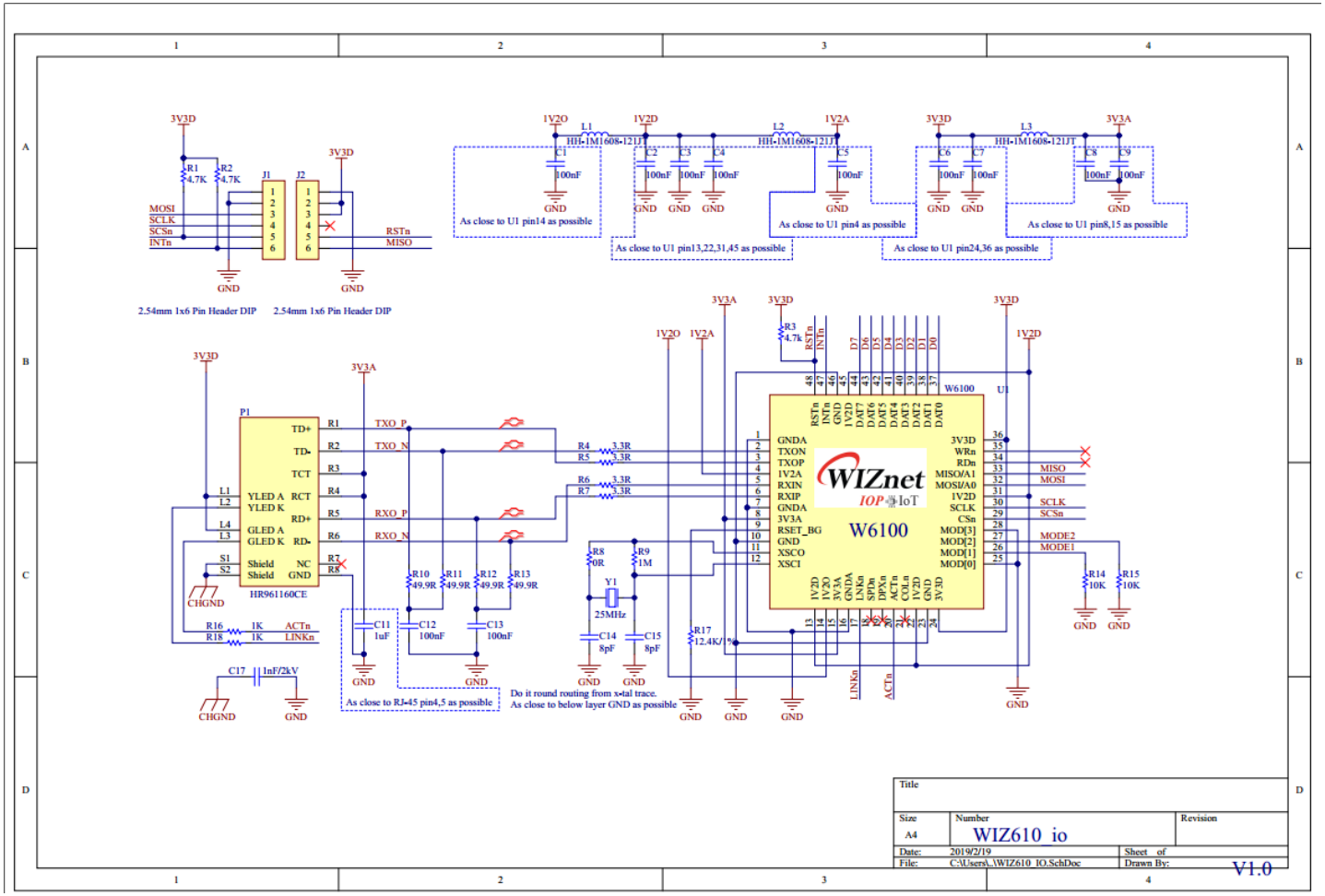
Symbol	Description	Min	Max	Units
F_{SCK}	SClK Clock Frequency		70	MHz
T_{CSS}	CSn Setup Time	3 SYS_CLK	-	ns
T_{CSH}	CSn Hold Time	2 SYS_CLK		ns
T_{CS}	CSn High Time	2 SYS_CLK		ns
T_{WH}	SCLK High time	3		ns
T_{WL}	SCLK Low Time	3		ns
T_{DS}	Data Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
TDI	Data Invalid Time	7		ns

5. Dimensions



6. Reference Schematics

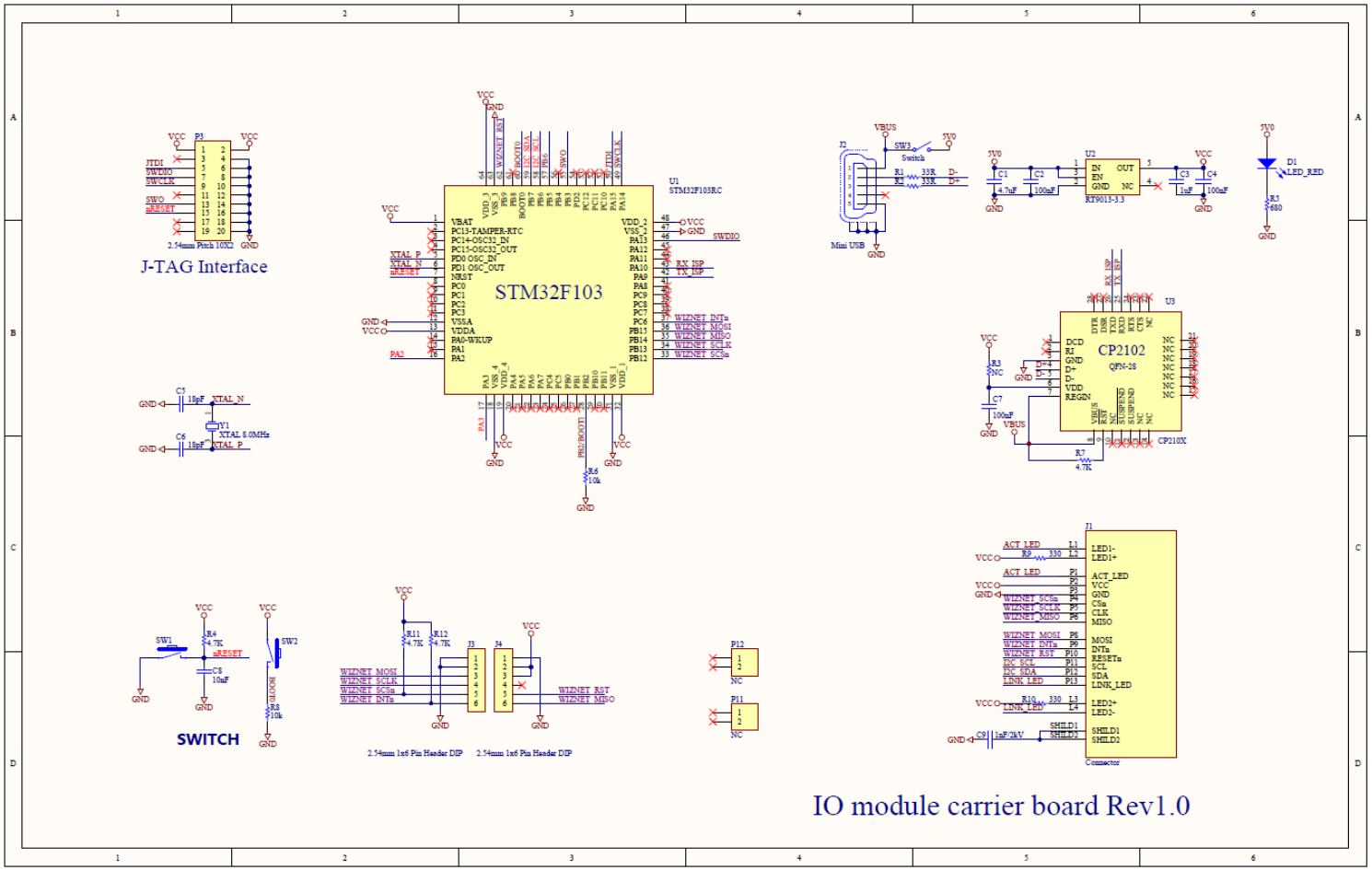
6.1.1 WIZ610IO Schematics



6.1.2 WIZ610IO Part List

Comment	Description	Designator	Footprint	Quantity
100nF	Ceramic CAP 0603(1608)	C1, C2, C3, C4, C5, C6, C7, C8, C9, C12, C13	0603-C	11
1uF	Ceramic CAP 0603(1608)	C11	0603-C	1
8pF	Ceramic CAP 0603(1608)	C14, C15	0603-C	2
1nF/2kV	Ceramic CAP 1808(4520)	C17	CAP-1206	1
2.54mm 1x6 Pin Header DIP	2.54mm 1x6 Pin Header DIP	J1, J2	IDC-1X6	2
120R FB	Inductor 0603(1608)	L1, L2, L3	0603-L	3
HR961160CE		P1	RJ-45(HR961160CE)	1
4.7K	RES0603	R1, R2, R3	0603-R	3
3.3R	RES0603	R4, R5, R6, R7	0603-R	4
0R	RES0603	R8	0603-R	1
1M	RES0603	R9	0603-R	1
49.9R	RES0603	R10, R11, R12, R13	0603-R	4
10K	RES0603	R14, R15	0603-R	2
1K	RES0603	R16, R18	0603-R	2
12K/1%	RES0603	R17	RES-0603	1
300/1%	RES0603	R19	RES-0603	1
W6100	WIZnet Hardwired TCP/IP Chip	U1	WIZNET W6100 QFN	1
25MHz	X-tal 25MHz,3.2x2.5 SMD	Y1	OSC-82J0626	1

6.2.1 IO Module Carrier Board Schematics



6.2.2 IO Module Carrier Board Part List

IO module carrier board Rev1.0_BOM			
Designator	Footprint	Quantity	Value
C1	0603-C	1	4.7uF
C2, C4	0603-C	2	100nF
C3	0603-C	1	1uF
C5, C6	0603-C	2	18pF
C7	0603-C	1	100nF
C8	0603-C	1	10nF
C9	1206-C	1	1nF/2kV
D1	0603-D	1	LED_RED
J2	USB-MINI-AB	1	Mini USB
J3, J4	IDC-1X6	2	2.54mm 1x6 Pin Header DIP
P11, P12	HDR1X2	2	NC
R1, R2	0603-R	2	33R
R3	0603-R	1	NC
R4, R7, R11, R12	0603-R	4	4.7K
R5	0603-R	1	680
R6, R8	0603-R	2	10k
R9, R10	0603-R	2	330
SW1, SW2	Button（6x6）	2	Button（6x6）
SW3	Switch（7x7）	1	Switch（7x7）
U1	QFP64(10mm x 10mm)	1	STM32F103RC
U2	SOT-23-5	1	RT9013-3.3
U3	QFN-28(5X5 0.5mm)	1	CP2102
Y1	3225	1	XTAL 8.0MHz

7. Warranty

WIZnet Co., Ltd. offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ610io module and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in Warranty.
3. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.io