DAVICOM Semiconductor, Inc.

DM9163

10/100 Mbps Fast Ethernet Physical Layer Single Chip Transceiver

DATA SHEET

Version: DM9163-16-MCO-DS-P01

August 20, 2014

Content

1 General Description

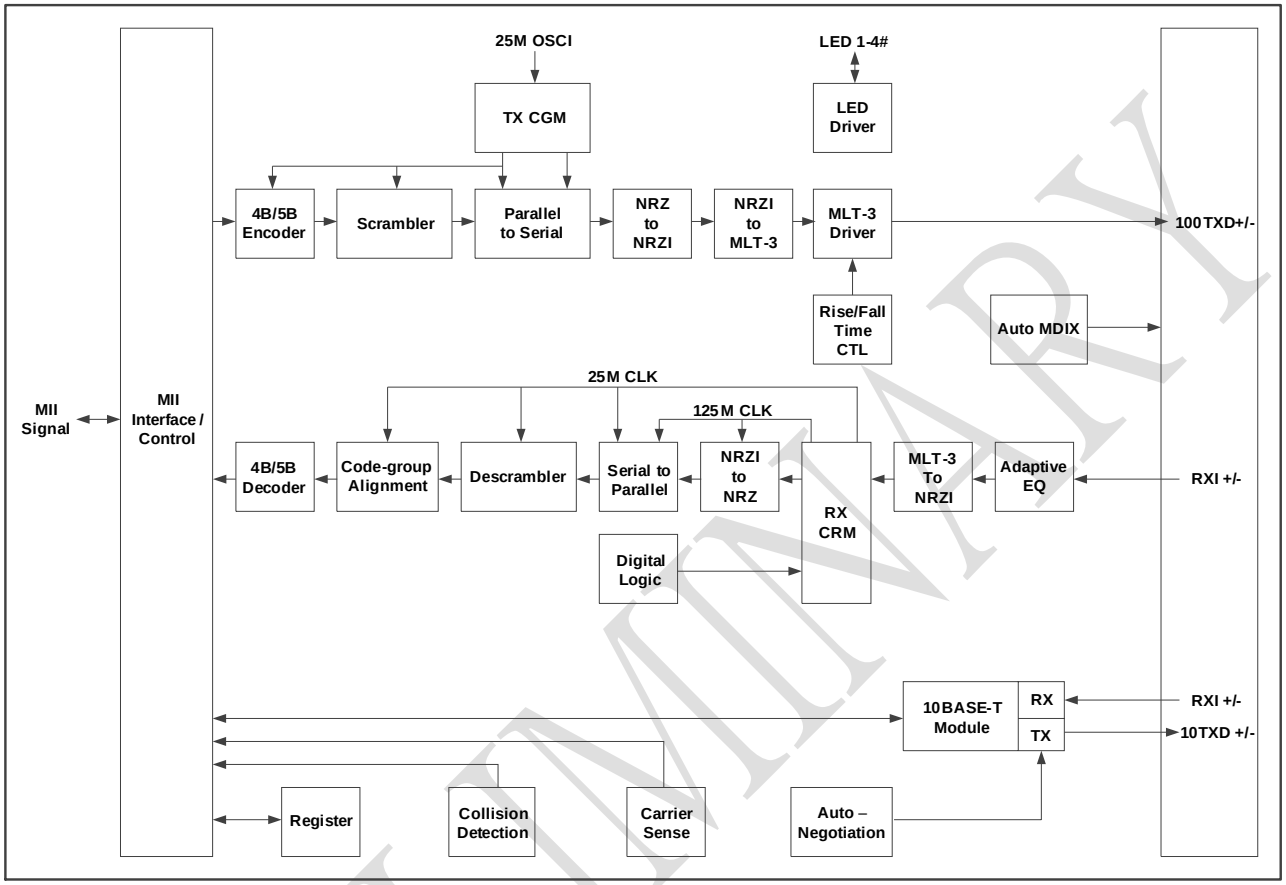
The DM9163 is a physical layer, single-chip with industrial temperature standard, and low power transceiver for 100BASE-TX and 10BASE-T operations. On the media side, it provides a direct interface to either Unshielded Twisted Pair Category 5 Cable (UTP5) for 100BASE-TX Fast Ethernet, or UTP5/UTP3 Cable for 10BASE-T Ethernet. Through the Media Independent Interface (MII), the DM9163 connects to the Medium Access Control (MAC) layer, ensuring a high interoperability from different vendors.

The DM9163 uses a low power and high performance advanced CMOS process. It contains the entire physical layer functions of 100BASE-TX as defined by IEEE802.3u, including the Physical Coding Sub-layer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sub-layer (TP-PMD), 10BASE-TX Encoder/Decoder (ENC/DEC), and Twisted Pair Media Access Unit (TPMAU). The DM9163 provides a strong support for the Auto-Negotiation function, utilizing automatic media speed and protocol selection. Furthermore, due to the built-in wave shaping filter, the DM9163 needs no external filter to transport signals to the media in 100BASE-TX or 10BASE-T Ethernet operation.

2 Features

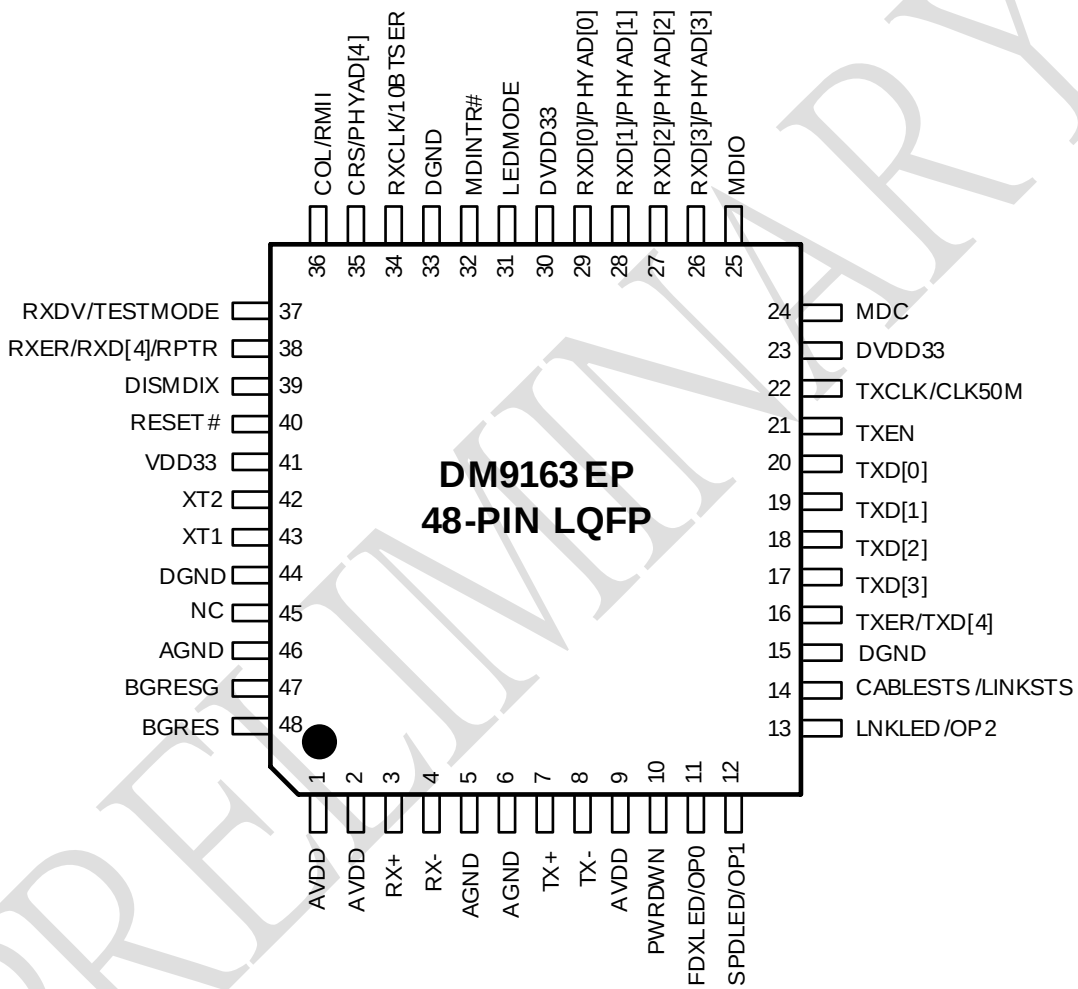
- **Fully complies with IEEE 802.3 / IEEE 802.3u 10Base-TX/ 100Base-TX, ANSI X3T12 TP-PMD1995 standards**
- **Support HP MDI/MDI-X auto crossover function (HP Auto-MDIX)**
- **Support Auto-Negotiation function, compliant with IEEE 802.3u**
- **Fully integrated Physical layer transceiver On-chip filtering with direct interface to magnetic transformer**
- **Selectable repeater or node mode**
- **Selectable MII or RMII (Reduced MII) mode for 100Base-TX and 10Base-TX**
- **Selectable MII or GPSI (7-Wired) mode for 10Base-TX**
- **Selectable Full-Duplex or Half-Duplex operation**
- **MII management interface with mask-able interrupt output capability**
- **Provide Loopback mode for easy system diagnostics**
- **LED status outputs indicate Link/ Activity, Speed10/100 and Full-Duplex/Collision**
- **Support Dual-LED optional control**
- **Support 50MHz clock output in RMII mode**
- **Single low power Supply of 3.3V with an advanced CMOS technology**
- **Support 3.3V transformer central tap**
- **Very Low Power consumption modes**
  - Power Reduced mode (cable detection)
  - Power Down mode
- **Compatible with 3.3V and 5.0V tolerant I/Os**
- **Support BIST function**
- **48-pin LQFP**

3 Block Diagram



4 Pin Configuration

4.1 48-Pin LQFP



5 Pin Description

Buffer Type		
I = Input	O = Output	LI = Latch input when power-up/reset
U = Pulled high	D= Pulled low	Z= Tri-State output

5.1 Normal MII Interface

Pin No.	Pin Name	I/O	Description
16	TXER/TXD [4]	I	Transmit Error/The Fifth TXD Data Bit In 100Mbps mode, when the signal indicates active high and TXEN is active, the HALT symbol substitutes the actual data nibble. In 10Mbps, the input is ignored In bypass mode (bypass BP4B5B), TXER becomes the TXD [4] pin, the fifth TXD data bit of the 5B symbol
20,19,18,17	TXD [0:3]	I	Transmit Data 4-bit nibble data inputs (synchronous to the TXCLK) when in 10/100Mbps nibble mode. In 10Mbps GPSI (7-Wired) mode, the TXD [0] pin is used as the serial data input pin, and TXD [1:3] are ignored.
21	TXEN	I	Transmit Enable Active high indicates the presence of valid nibble data on the TXD [0:3] for both 100Mbps and 10Mbps nibble modes. In 10Mbps GPSI (7-Wired) mode, active high indicates the presence of valid 10Mbps data on TXD [0].
22	TXCLK/ CLK50M	O,Z,LI,(D)	Transmit Clock The transmitting clock provides the timing reference for the transfer of the TXEN, TXD, and TXER. TXCLK is provided by the PHY When in Normal MII mode: 25MHz in 100Mbps nibble mode, 2.5MHz in 10Mbps nibble mode, 10MHz in 10Mbps GPSI (7-Wired) mode ISOLATE Setting: (When power up reset, latch input) 1 = Reg 0.10 will be initialized to “1”. When in Reduced MII mode and this pin is latched high at the end of reset: This pin is the 50MHz clock output after the end of reset 0 = Reg 0.10 will be initialized to “0”. (Ref.to 8.1 Basic Control Register)
24	MDC	I	Management Data Clock Synchronous clock for the MDIO management data. This clock is provided by management entity, and it is up to 2.5MHz
25	MDIO	I/O	Management Data I/O Bi-directional management data which may be provided by the station management entity or the PHY
29,28,27,26	RXD[0:3]/ PHYAD[0:3]	O,Z,LI,(D)	Receive Data Output 4-bit nibble data outputs (synchronous to RXCLK) when in 10/100Mbps MII mode In 10Mbps GPSI (7-Wired) mode, the RXD [0] pin is used as the serial data output pin, and the RXD [1:3] are ignored PHY address [0:3] (power up reset latch input) PHY address sensing input pins.

32	MDINTR#	IO,LI,(D)	Status Interrupt Output: Whenever there is a status change (link, speed, duplex depend on interrupt register [21]) The interrupt output assert low when pull up. Asserted high when pull down.
34	RXCLK/ 10BTSER	O,Z,LI,(U)	Receive Clock The received clock provides the timing reference for the transfer of the RXDV, RXD, and RXER. RXCLK is provided by PHY. The PHY may recover the RXCLK reference from the received data or it may derive the RXCLK reference from a nominal clock 25MHz in 100Mbps MII mode, 2.5MHz in 10Mbps MII mode, 10MHz in 10Mbps GPSI (7-Wired) mode 10BTSER only support for 10M mode; (power up reset latch input) 1 = MII mode in 10M mode 0 = GPSI (7-Wired) mode in 10M mode
35	CRS/ PHYAD[4]/	O,Z,LI,(D)	Carrier Sense Detect/ PHYAD[4] Asserted high to indicate the presence of carrier due to receive or transmit activities in Half-Duplex mode of 10BASE-T or 100BASE-TX. In repeater mode or Full-Duplex mode, this signal is asserted high to indicate the presence of carrier due to receive activity only This pin is also used as PHYAD [4] (power up reset latch input) PHY address sensing input pin.
36	COL/ RMII	O,Z,LI,(D)	Collision Detection Asserted high to indicate the detection of the collision conditions in Half-Duplex mode of 10Mbps and 100Mbps. In Full-Duplex mode, this signal is always logical 0 Reduced MII enable: This pin is also used to select Normal MII or Reduced MII. (power up reset latch input) 1= Reduced MII This pin is always pulled low except used as reduced MII 0= Normal MII (default)
37	RXDV/ TESTMODE	O,Z,LI,(D)	Receive Data Valid Asserted high to indicate that the valid data is presented on the RXD [0:3] Test mode control pin (power up reset latch input) 1 = Enable test mode 0 = Normal operation (default)
38	RXER/RXD[4]/ RPTR	O,Z,LI,(D)	Receive Data Error/The Fifth RXD Data Bit of the 5B Symbol Asserted high to indicate that an invalid symbol has been detected In decoder bypass mode (bypass BP4B5B), RXER becomes RXD [4], the fifth RXD data bit of the 5B symbol This pin is also used to select Repeater or Node mode. (power up reset latch input) 1 = Repeater Mode 0 = Node Mode (default)
31	LEDMODE	I	LED MODE Select Reference LED function description 1 = Normal LED 0 = Support Dual-LED
40	RESET#	I	Reset Active low input that initializes the DM9163.

5.2 Media Interface

Pin No.	Pin Name	I/O	Description
3,4	RX+ RX-	I/O	Differential Receive Pair Differential data is received from the media Note: the central tap of transformer is 3.3V
7,8	TX+ TX-	I/O	Differential Transmit Pair/PECL Transmit Pair Differential data is transmitted to the media in TP mode Note: the central tap of transformer is 3.3V

5.3 LED Interface

Pin No.	Pin Name	I/O	Description
11	FDXLED/ OP0	O,LI,(U)	Full-Duplex LED output OP0: (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9163 according to the Table A. The value is latched into the DM9163 registers at power-up/reset
12	SPDLED/ OP1	O,LI,(U)	Speed LED output OP1: (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9163 according to the Table A. The value is latched into the DM9163 registers at power-up/reset
13	LNKLED/ OP2	O,LI,(U)	Link LED output OP2: (power up reset latch input) This pin is used to control the forced or advertised operating mode of the DM9163 according to the Table A. The value is latched into the DM9163 registers at power-up/reset

5.4 Mode

Pin No.	Pin Name	I/O	Description
10	PWRDWN	I	Power Down Control Asserted high to force the DM9163 into power down mode. When in power down mode, most of the DM9163 circuit block's power is turned off, only the MII management interface (MDC, MDIO) logic is available (the PHY should respond to management transactions and should not generate spurious signals on the MII)). To leave power down mode, the DM9163 needs the hardware or software reset with the PWRDWN pin low
14	CABLESTS/ LINKSTS	O,LI,(D)	Cable Status or Link Status This pin is used to indicate the status of the cable connection when power up reset latch low (Default) 1 = With cable connection 0 = Without cable connection This pin is used to indicate the status of the Link connection when power up reset latch high 1 = Without link 0 = With link
39	DISMDIX	I,(D)	HP Auto-MDIX Control 1 = Disable Auto mode 0 = Enable HP Auto-MDIX mode
45	NC		

5.5 Bias and Clock

Pin No.	Pin Name	I/O	Description
43,42	XT1,XT2	I/O	Reference Clock Input When in Normal MII mode or when in Reduced MII mode and pin TXCLK is latched high at the end of reset: A 25MHz crystal or oscillator as DM9163 reference clock is used. If the crystal is used, it is connected across pins XT1 and XT2. If the oscillator is used, it can either connect to pin XT1 (left pin XT2 unconnected) or to pin XT2 (left pin XT1 unconnected). When in Reduced MII mode and pin TXCLK is latched low at the end of reset: A 50MHz oscillator is used, and it can either connect to pin XT1 (left pin XT2 unconnected) or to pin XT2 (left pin XT1 unconnected).
47	BGRESG	P	Band gap Ground
48	BGRES	O	Band gap Voltage Reference Resistor 6.98K ohm +/- 1%

5.6 Power

Pin No.	Pin Name	I/O	Description
1,2,9	AVDD	P	Analog 1.8V Regulator Power output
5	AGND	P	Analog Receive Ground
6	AGND	P	Analog Transmit Ground
15,33,44	DGND	P	Digital Ground
23,30	DVDD33	P	Digital Power
41	VDD33	P	Digital Power for Crystal
46	AGND	P	Analog Substrate Ground

5.7 Table (Media Type Selection)

OP2	OP1	OP0	Function
0	0	0	Dual Speed 100/10 HDX
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Manually Select 10TX HDX
1	0	0	Manually Select 10TX FDX
1	0	1	Manually Select 100TX HDX
1	1	0	Manually Select 100TX FDX
1	1	1	Auto-Negotiation Enables All Capabilities

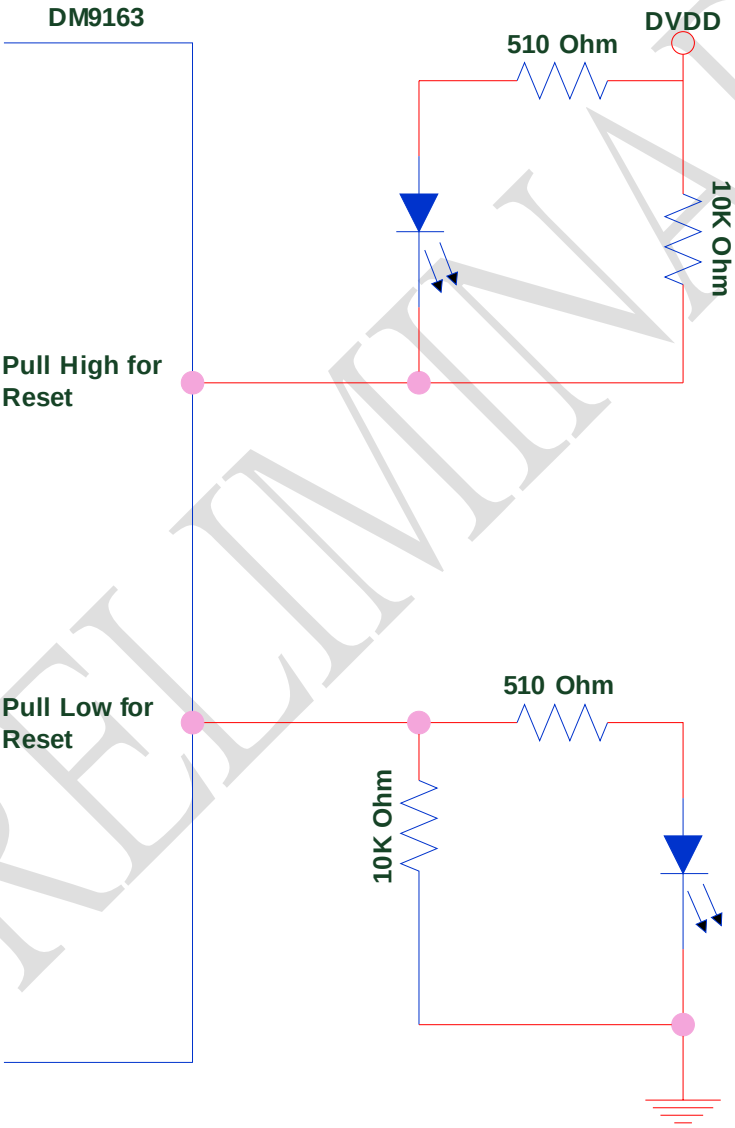
5.8 Pin Maps of Normal MII, Reduced MII, and 10Base-T GPSI (7-Wired) Mode

Pin No.	Normal MII Mode	Reduced MII Mode	10Base-T GPSI (7-Wired) Mode
16	TXER/TXD [4]	NC	NC
18,17	TXD [2:3]	NC	NC
20,19	TXD [0:1]	TXD [0:1]	TXD [0] ; TXD [1] = NC
21	TXEN	TXEN	TXEN
22	TXCLK	NC	TXCLK
24	MDC	MDC	MDC
25	MDIO	MDIO	MDIO
27,26	RXD[2:3]	NC	NC
29,28	RXD [0:1]	RXD [0:1]	RXD [0] ; RXD [1] = NC
34	RXCLK	NC	RXCLK
35	CRS (PHYADR [4]) (BP4B5B)	NC	CRS
36	COL	NC	COL
37	RXDV	CRS DV	NC
38	RXER/RXD[4]/RPTR/NODE	RPTR/NODE	RPTR/NODE
40	RESET#	RESET#	RESET#
43	XT1 (25 MHz)	XT1 or XT2 (REF_CLK 50MHz)*	XT1 (25 MHz)

*Note: Please see 5.5 Bias and Clock for detail connection – P10

6 LED Configuration

LEDs flash once per 500ms after power-on reset or software reset by writing PHY register. All LED pins are dual function pins, which can be configured as either active high or low by pulling them low or high accordingly. If the pin is pulled high, the LED is active low after reset. Likewise, if the pin is pulled low, the LED is active high. LEDs flash once per 500ms after power-on reset or software reset by writing PHY register. All LED pins are dual function pins, which can be configured as either active high or low by pulling them low or high accordingly. If the pin is pulled high, the LED is active low after reset. Likewise, if the pin is pulled low, the LED is active high.



6.1 LED Function Description

Normal LED mode

LED_MODE = 1					
Name	Pin	Lo	Hi	Lo	Hi
LED0	11	FDX	HDX	FDX	HDX
LED1	12	SPEED: 100M	SPEED: 10M	SPEED: 100M	SPEED: 10M
CABLESTS / LINKSTS		Pull Down		Pull Up	
Name	Pin	Lo	Hi	Lo	Hi
LED2	13	Link	Link Fail	N/A	
		Flashing (HiLo) Active		Flashing (HiLo) Active	
CABLESTS / LINKSTS	14	Without Cable connection	With Cable connection	With Link	Without Link

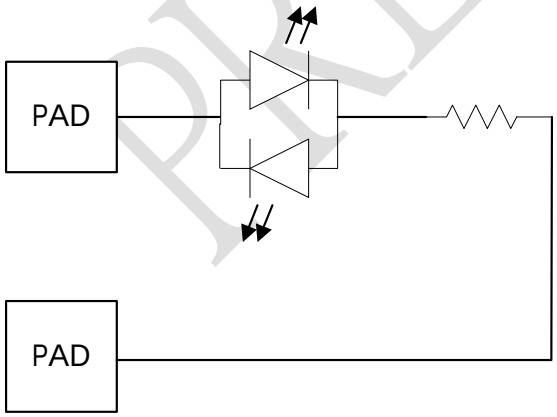
*48pin-LQFP: Pin 31 = LEDMODE

For Dual-LED

LED_MODE = 0						
Name	Pin	LINK Mode				
		Link Fail	SPEED: 100M		SPEED: 10M	
			Link OK	Active	Link OK	Active
LED0	11	Lo	Lo	Flashing (LoHi)	HI	Flashing (HiLo)
LED1	12	Lo	Hi		Lo	
CABLESTS / LINKSTS		Pull Down		Pull Up		
Name	Pin	Lo	Hi	Lo	Hi	
LED2	13	FDX	HDX	FDX	HDX Flashing (LoHi) Collision	
CABLESTS / LINKSTS	14	Without Cable connection	With Cable connection	With Link	Without Link	

* Pin 31 = LEDMODE

6.1.1 Dual-LED Application Circuit



7 Function Description

The DM9163 Fast Ethernet single chip transceiver, providing the functionality as specified in IEEE 802.3u, integrates a complete 100Base-TX module and a complete 10Base-T module. The DM9163 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The DM9163 performs all PCS (Physical Coding Sub layer), PMA (Physical Media Access), TP-PMD (Twisted Pair Physical Medium Dependent) sub layer, 10Base-T Encoder/Decoder, and Twisted Pair Media Access Unit (TPMAU) functions. Figure 7-1 shows the major functional blocks implemented in the DM9163.

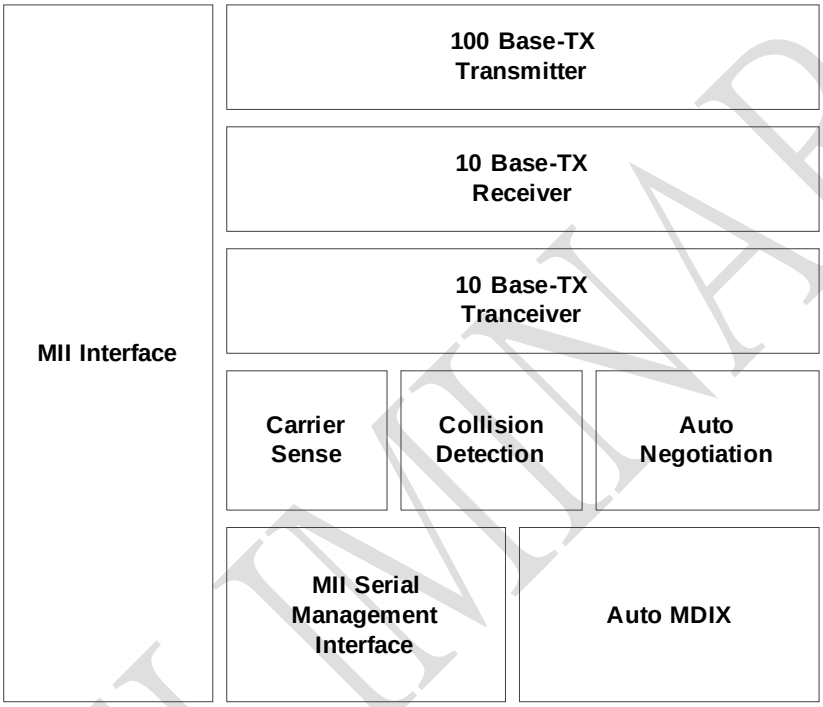


Figure 7-1

7.1 MII Interface

The DM9163 provides a Media Independent Interface (MII) as defined in the IEEE 802.3u standard (Clause 22).

The purpose of the MII interface is to provide a simple, easy to implement connection between the MAC Reconciliation layer and the PHY. The MII is designed to make the differences between various media transparent to the MAC sub layer.

The MII consists of a nibble wide receive data bus, a nibble wide transmit data bus, and control signals to facilitate data transfers between the PHY and the Reconciliation layer.

- TXD (transmit data) is a nibble (4 bits) of data that are driven by the reconciliation sub layer synchronously with respect to TXCLK. For each TXCLK period, which TXEN is asserted, TXD (3:0) are accepted for transmission by the PHY.
- TXCLK (transmit clock) output to the MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the TXEN, TXD, and TXER signals.
- TXEN (transmit enable) input from the MAC reconciliation sub layer indicates that nibbles are being presented on the MII for transmission on the physical medium.
- TXER (transmit coding error) transitions are synchronously with respect to TXCLK. If TXER is asserted for one or more clock periods, and TXEN is asserted, the PHY will emit one or more symbols that are not part of the valid data delimiter set somewhere in the frame being transmitted.
- RXD (receive data) is a nibble (4 bits) of data that are sampled by the reconciliation sub layer synchronously with respect to RXCLK. For each RXCLK period which RXDV is asserted, RXD (3:0) are transferred from the PHY to the MAC reconciliation sub layer.
- RXCLK (receive clock) output to the MAC reconciliation sub layer is a continuous clock that provides the timing reference for the transfer of the RXDV, RXD, and RXER signals.
- RXDV (receive data valid) input from the PHY indicates that the PHY is presenting recovered and decoded nibbles to the MAC reconciliation sub layer. To interpret a receive frame correctly by the reconciliation sub layer, RXDV must encompass the frame, starting no later than the Start-of-Frame delimiter and excluding any End-Stream delimiter.
- RXER (receive error) transitions are synchronously with respect to RXCLK. RXER will be asserted for 1 or more clock periods to indicate to the reconciliation sub layer that an error was detected somewhere in the frame being transmitted from the PHY to the reconciliation sub layer.
- CRS (carrier sense) is asserted by the PHY when either the transmit or receive medium is non-idle, and de-asserted by the PHY when the transmit and receive medium are idle. Figure 7-2 depicts the behavior of CRS during 10Base-T and 100Base-TX transmission.

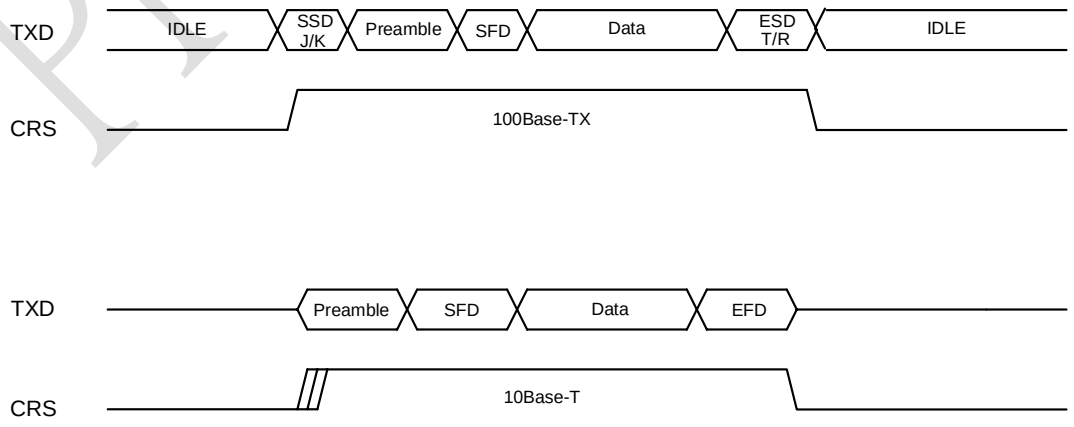


Figure 7-2

7.2 100Base –TX Operation

The 100Base-TX transmitter receives 4-bit nibble data clocked in at 25MHz at the MII, and outputs a scrambled 5-bit encoded MLT-3 signal to the media at 100Mbps. The on-chip clock circuit converts the 25MHz clock into a 125MHz clock for internal use.

The IEEE 802.3u specification defines the Media Independent Interface. The interface specification defines a dedicated receive data bus and a dedicated transmit data bus.

These two busses include various controls and signal indications that facilitate data transfers between the DM9163 and the Reconciliation layer.

7.2.1 100Base-TX Transmit

The 100Base-TX transmitter consists of the functional blocks shown in figure 7-3. The 100Base-TX transmit section converts 4-bit synchronous data provided by the MII to a scrambled MLT-3 125, a million symbols per second serial data stream.

The block diagram in figure 7-3 provides an overview of the functional blocks contained in the transmit section.

The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Encoder
- NRZI to MLT-3
- MLT-3 Driver

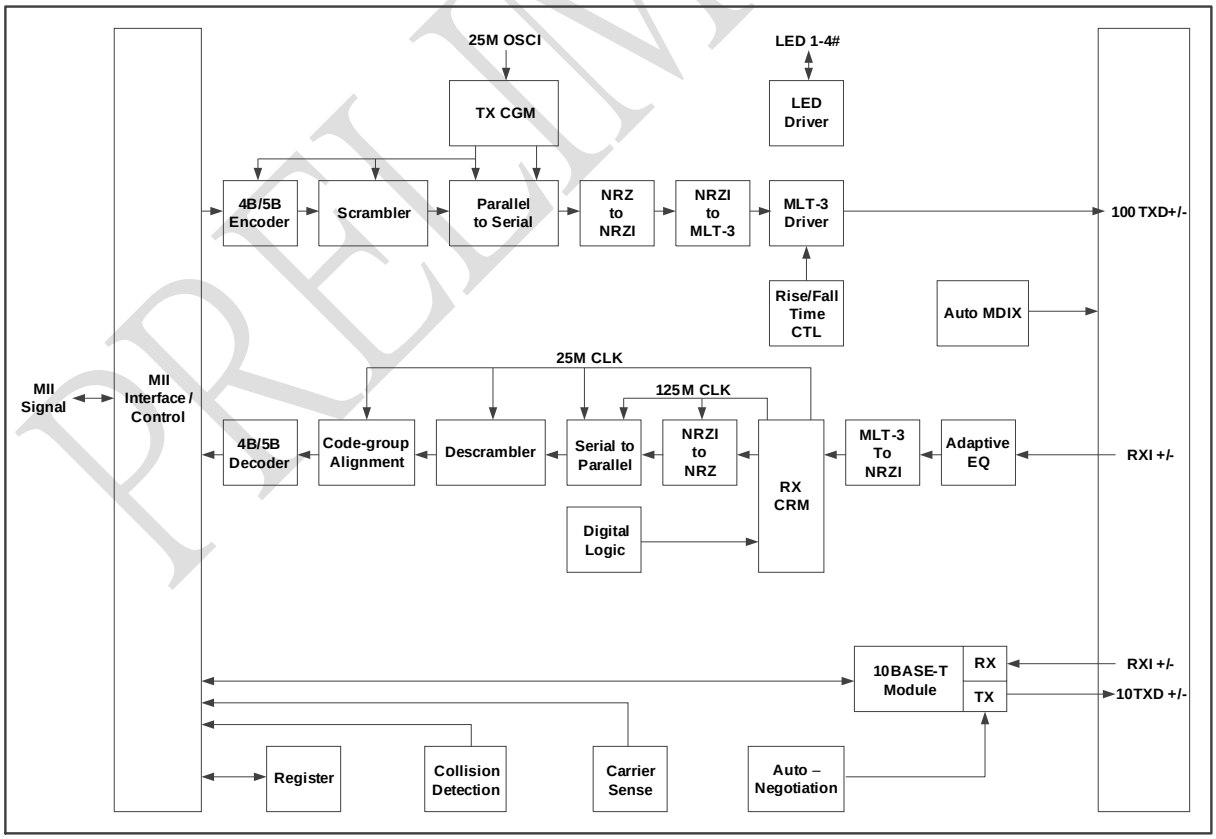


Figure 7-3

7.2.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, see reference Table 7-1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code group pair (01101 00111) indicating end of frame. After the T/R code group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9163 includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters, which do not require 4B5B conversion.

7.2.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

7.2.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI encoder block.

7.2.1.4 NRZ to NRZI Encoder

Since the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

7.2.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

7.2.1.6 MLT-3 Driver

The two binary data streams, created at the MLT-3 converter, are fed to the twisted pair output driver, which converts these streams to current sources and alternately drives either side of the transmit transformed at the MLT-3 converter, are fed to the twisted pair output driver, which converts these streams to current sourcMLT-3 converter.

7.2.1.7 4B5B Cod3 Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 7-1

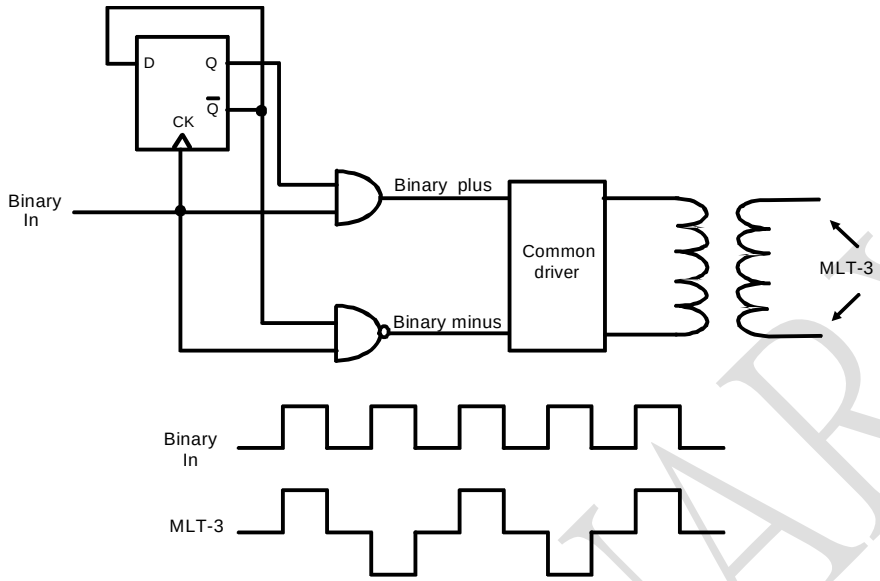


Figure 7-4

7.2.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data, which is then provided to the MII.
The receive section contains the following functional blocks:

- Signal Detect
- Adaptive Equalizer
- MLT-3 to NRZI Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

7.2.2.1 Signal Detect

The signal detects function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX Standards for both voltage thresholds and timing parameters.

7.2.2.2 Adaptive Equalizer

When transmitting data at high speeds over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation requires significant compensation, which will be over-kill in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

7.2.2.3 MLT-3 to NRZI Decoder

The DM9163 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relation between NRZI and MLT-3 data is shown in figure 7-4.

7.2.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125MHz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

7.2.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

7.2.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

7.2.2.7 Descrambler

Because the scrambling process requires to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

7.2.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected and subsequent data is aligned on a fixed boundary.

7.2.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first 2 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols). The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

7.2.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9163 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented to the MII interface in nibble format, converted to a serial bit stream, then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted into nibble format for presentation to the MII interface.

7.2.4 Collision Detection

For Half-Duplex operation, a collision is detected when transmit and receive channels are active simultaneously. When a collision has been detected, it will be reported by the COL signal on the MII interface. Collision detection is disabled in Full-Duplex operation.

7.2.5 Carrier Sense

Carrier Sense (CRS) is asserted in Half-Duplex operation during transmission or reception of data. During Full-Duplex mode, CRS is asserted only during receive operations

7.2.6 Auto-Negotiation

The objective of Auto-Negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-Negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.
Auto-Negotiation also provides a parallel detection function for devices that do not support the Auto-Negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology, supported by the receiving device, a connection will be automatically established using that technology. This allows devices, which do not support Auto-Negotiation but support a common mode of operation, to establish a link.

7.2.7 MII Serial Management

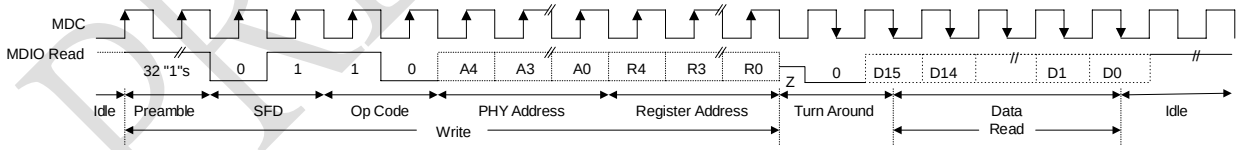
The MII serial management interface consists of a data interface, basic register set, and a serial management interface to the register set. Through this interface it is possible to control and configure multiple PHY devices, get status and error information, and determine the type and capabilities of the attached PHY device(s).
The DM9163 management functions correspond to MII specification for IEEE 802.3u-1995 (Clause 22) for registers 0 through 6 with vendor-specific registers 16, 17, 18, 21, 22, 23 and 24.

In read/write operation, the management data frame is 64-bits long and starts with 32 contiguous logic one bits (preamble) synchronization clock cycles on MDC. The Start of Frame Delimiter (SFD) is indicated by a <01> pattern followed by the operation code (OP) :< 10> indicates Read operation and <01> indicates Write operation. For read operation, a 2-bit turnaround (TA) filing between Register Address field and Data field is provided for MDIO to avoid contention. Following the turnaround time, 16-bit data is read from or written onto management registers.

7.2.8 Serial Management Interface

The serial control interface uses a simple two-wired serial interface to obtain and control the status of the physical layer through the MII interface. The serial control interface consists of MDC (Management Data Clock), and MDI/O (Management Data Input/Output) signals. The MDIO pin is bi-directional and may be shared by up to 32 devices.

7.2.9 Management Interface - Read Frame Structure



7.2.10 Management Interface - Write Frame Structure

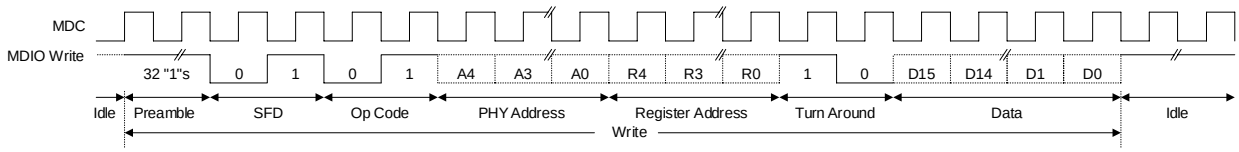


Figure 7-5

7.2.11 Power Reduced Mode

The Signal detect circuit is always turned on to monitor whether there is any signal on the media. In case of cable disconnection, DM9163 will automatically turn off the power and enter the Power Reduced mode, regardless of its operation mode being N-way Auto-Negotiation or forced mode. While in the Power Reduced mode, the transmit circuit will continue sending out fast link pulse with minimum power consumption. If a valid signal is detected from the media, which might be N-way fast link pulse, 10Base-T normal link pulse, or 100Base-TX MLT3 signals, the device wakes up and resumes normal operation mode.

Automatic reduced power down mode can be disabled by writing Zero to Reg.16.4.

7.2.12 Power Down Mode

Power Down mode is entered by setting Reg.0.11 to ONE or pulling PWRDWN pin high, which disables all transmit and receive functions, and MII interface functions except the MDC/MDIO management interface.

7.2.13 Reduced Transmit Power Mode

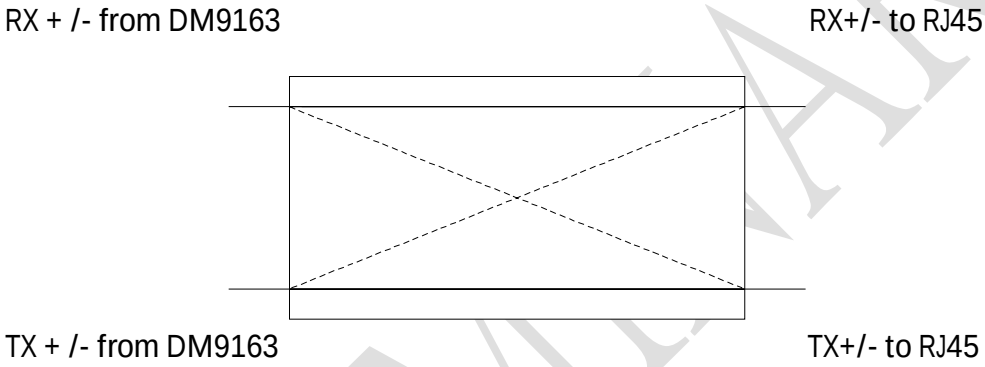
Additional transmit power reduction can be gained by designing with 1.25:1 turns ration magnetic on its TX side and using a 8.7K ohms resistor on BGRES pin, and the TX+/TX- pulled high resistors being changed from 50ohms to 78 ohms. This configuration could reduced about 20% of transmit power.

7.3 HP Auto-MDIX Functional Descriptions

The DM9163 supports the automatic detect cable connection type, MDI/MDIX (straight through/cross over). A manual configuration by register bit for MDI or MDIX is still accepted.

When set to automatic, the polarity of MDI/MDIX controlled timing is generated by 16-bits LFSR. The switching cycle time is located from 200ms to 420ms. The polarity control is always switch until detect received signal. After selected MDI or MDIX, the polarity status can be read by register bit (20.7). (See page33, 8.12 specified config register-20 bit 7) 7.3.1 Function Setting. Pin 39 is used to enable HP Auto-MDIX function.

Pull pin 39 low will enable it, and pull pin 39 high will disable it. Specified config Register 20 bit 4 (20, 4) is used by programmer to disable HP Auto-MDIX function. Write register 20 bit 4 to “1“ will disable HP Auto-MDIX function. Its default value is “0“. When the register 20 bit 4 (20, 4) is set to “1“, the register 20 bit 5(20, 5) is used to select straight through or cross over mode, “0“ for straight through, and “1“ for cross over.



* MDI: _____

* MDIX: - - - - - - - - -

This feature is able to detect the required cable connection type. (Straight through or crossed over) and make correction automatically

8 MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop Back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
		0	0	1	1	0	0	0	1	0	000_0000						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
								001010					0000				
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
16	Specified Config	BP 4B5B	BP SCR	BP ALIGN	BP_ ADPOK	Repeater	TX	FEF_EN	RMII_EN	Force 100LNK	TST_ SEL0	LEDCOL_ SEL	RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Specified Conf/Sta	100 FDX	100 HDX	10 FDX	10 HDX	Reserved	Reserved	Reserved	PHY ADDR [4:0]					Auto-N. Monitor Bit [3:0]			
18	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	10T Serial	Reserved									Polarity Reverse
19	PWDOR	Reserved							PD10DRV	PD100l	PDchip	PDcrm	PDaeq	PDdrv	PDecli	PDeclo	PD10
20	Specified Config	TSTSE1	TSTSE2	FORCE_ TXSD	FORCE_ FEF	PREAM BLEX	TX10M_ PWR	NWAY_ PWR	Reserved	MDIX_ CNTL	AutoNeg_ dlpbk	Mdix_fix Value	Mdix_ down	MonSel1	MonSel0	Rmii_ accu	PD_ value
21	MDINTR	Int_sts	Reserved	Reserved	Reserved	Fdx_msk	Spd_msk	Lnk_msk	Int_msk	Reserved	Reserved	Reserved	Fdx_chg	Spd_chg	Lnk_chg	Reserved	Int_sts
22	RCVER	Receiver Error Counter															
23	DIS_connect	Reserved								Disconnect_counter							
24	RSTLH	Lh_led_ mode	Lh_ mdintr	Lh_ cabsts	Lh_ isolate	Lh_rmii	Lh_seril10	Lh_ repeater	Lh_ testmode	Lh_op2	Lh_op1	Lh_op0	Lh_ phyad4	Lh_ phyad3	Lh_ phyad2	Lh_ phyad1	Lh_ phyad0
25	RADVR	Reserved															
26	RLPAR	Reserved															
27	DSPCR	Reserved															
28	CABCR	Reserved		DLY_ INV	DLY_50M	Reserved	Reserved						Reserved			Cable Control	
29	PSCR	bist_start	bist_status	bist_i_l	Reserved	preamblex	Reserved	TX_PWR	Reserved								

Key to Default

In the register description that follows, the default column takes the form:

<Reset Value>:
- 1 Bit set to logic one
- 0 Bit set to logic zero
- X No default value
- (PIN#) Value latched in from pin # at reset

<Access Type>:
- RO = Read only
- RW = Read/Write

<Attribute(s)>:
SC = Self clearing
P = Value permanently set
LL = Latching low
LH = Latching high

8.1 Basic Mode Control Register (BMCR) - 00

Bit	Bit Name	Default	Description
0.15	Reset	0,RW/SC	Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0,RW	Loopback Loop-back control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appears at the MII receive outputs
0.13	Speed selection	1,RW	Speed Select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by Auto-Negotiation. When Auto-Negotiation is enabled and bit 12 is set, this bit will return Auto-Negotiation selected medium type
0.12	Auto-Negotiation enable	1,RW	Auto-Negotiation Enable 1 = Auto-Negotiation is enabled, bit 8 and 13 will be in Auto-Negotiation status
0.11	Power down	0,RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII 1=Power down 0=Normal operation
0.10	Isolate	0,RW	Isolate 1 = Isolates the DM9163 from the MII with the exception of the serial management. (When this bit is asserted, the DM9163 does not respond to the TXD [0:3], TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD [0:3], COL and CRS outputs. When PHY is isolated from the MII it shall respond to the management transactions) 0 = Normal operation
0.9	Restart Auto-Negotiation	0,RW/SC	Restart Auto-Negotiation 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. When Auto-Negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning to a value of 1 until Auto-Negotiation is initiated by the DM9163. The operation of the Auto-Negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation

0.8	Duplex mode	1,RW	Duplex Mode 1 = Full-Duplex operation. Duplex selection is allowed when Auto-Negotiation is disabled (bit 12 of this register is cleared). With Auto-Negotiation enabled, this bit reflects the duplex capability selected by Auto-Negotiation 0 = Normal operation
0.7	Collision test	0,RW	Collision Test 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0 = Normal operation
0.6:0.0	RESERVED	0,RO	Reserved Read as 0, ignore on write

8.2 Basic Mode Status Register (BMSR) – 01

Bit	Bit Name	Default	Description
1.15	100BASE-T4	0,RO/P	100BASE-T4 Capable 1 = DM9163 is able to perform in 100BASE-T4 mode 0 = DM9163 is not able to perform in 100BASE-T4 mode
1.14	100BASE-TX Full-Duplex	1,RO/P	100BASE-TX Full-Duplex Capable 1 = DM9163 is able to perform 100BASE-TX in Full-Duplex mode 0 = DM9163 is not able to perform 100BASE-TX in Full-Duplex mode
1.13	100BASE-TX Half-Duplex	1,RO/P	100BASE-TX Half-Duplex Capable 1 = DM9163 is able to perform 100BASE-TX in Half-Duplex mode 0 = DM9163 is not able to perform 100BASE-TX in Half-Duplex mode
1.12	10BASE-T Full-Duplex	1,RO/P	10BASE-T Full-Duplex Capable 1 = DM9163 is able to perform 10BASE-T in Full-Duplex mode 0 = DM9163 is not able to perform 10BASE-TX in Full-Duplex mode
1.11	10BASE-T Half-Duplex	1,RO/P	10BASE-T Half-Duplex Capable 1 = DM9163 is able to perform 10BASE-T in Half-Duplex mode 0 = DM9163 is not able to perform 10BASE-T in Half-Duplex mode
1.10:1.7	RESERVED	0,RO	Reserved Read as 0, ignore on write
1.6	MF preamble suppression	1,RO	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
1.5	Auto-Negotiation Complete	0,RO	Auto-Negotiation Complete 1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed
1.4	Remote fault	0,RO/LH	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is DM9163 implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected

1.3	Auto-Negotiation ability	1,RO/P	Auto Configuration Ability 1 = DM9163 is able to perform Auto-Negotiation 0 = DM9163 is not able to perform Auto-Negotiation
1.2	Link status	0,RO/LL	Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation) 0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber detect	0,RO/LH	Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a DM9163 reset. This bit works only in 10Mbps mode
1.0	Extended capability	1,RO/P	Extended Capability 1 = Extended register capable 0 = Basic register capable only

8.3 PHY ID Identifier Register #1 (PHYID1) - 02

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9163. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
2.15:2.0	OUI_MSB	<0181h>	OUI Most Significant Bits This register stores bit 3 to 18 of the OUI (00606E) to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

8.4 PHY ID Identifier Register #2 (PHYID2) - 03

Bit	Bit Name	Default	Description
3.15:3.10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9:3.4	VNDR_MDL	<001010>, RO/P	Vendor Model Number Five bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3:3.0	MDL_REV	<0000>, RO/P	Model Revision Number Five bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 4)

8.5 Auto-Negotiation Advertisement Register (ANAR) – 04

This register contains the advertised abilities of this DM9163 device as they will be transmitted to its link partner during Auto-Negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	Next page Indication 1 = Next page available 0 = No next page available The DM9163 has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9163's Auto-Negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the Auto-Negotiation process. Software should not attempt to write to this bit.
4.13	RF	0,RW	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
4.12:4.11	RESERVED	X,RW	Reserved Write as 0, ignore on read
4.10	FCS	0,RW	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
4.9	T4	0,RO/P	100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The DM9163 does not support 100BASE-T4 so this bit is permanently set to 0
4.8	TX_FDX	1,RW	100BASE-TX Full-Duplex Support 1 = 100BASE-TX Full-Duplex is supported by the local device 0 = 100BASE-TX Full-Duplex is not supported
4.7	TX_HDX	1,RW	100BASE-TX Support 1 = 100BASE-TX Half-Duplex is supported by the local device 0 = 100BASE-TX Half-Duplex is not supported
4.6	10_FDX	1,RW	10BASE-T Full-Duplex Support 1 = 10BASE-T Full-Duplex is supported by the local device 0 = 10BASE-T Full-Duplex is not supported
4.5	10_HDX	1,RW	10BASE-T Support 1 = 10BASE-T Half-Duplex is supported by the local device 0 = 10BASE-T Half-Duplex is not supported
4.4:4.0	Selector	<00001>,RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

8.6 Auto-Negotiation Link Partner Ability Register (ANLPAR) – 05

This register contains the advertised abilities of the link partner when received during Auto-Negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0,RO	Next Page Indication 1 = Link partner, next page available 1 = Link partner, next page available
5.14	ACK	0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The DM9163's Auto-Negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
5.13	RF	0,RO	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
5.12:5.11	RESERVED	0,RO	Reserved Read as 0, ignore on write
5.10	FCS	0,RO	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
5.9	T4	0,RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
5.8	TX_FDX	0,RO	100BASE-TX Full-Duplex Support 1 = 100BASE-TX Full-Duplex is supported by the link partner 0 = 100BASE-TX Full-Duplex is not supported by the link partner
5.7	TX_HDX	0,RO	100BASE-TX Support 1 = 100BASE-TX Half-Duplex is supported by the link partner 0 = 100BASE-TX Half-Duplex is not supported by the link partner
5.6	10_FDX	0,RO	10BASE-T Full-Duplex Support 1 = 10BASE-T Full-Duplex is supported by the link partner 0 = 10BASE-T Full-Duplex is not supported by the link partner
5.5	10_HDX	0,RO	10BASE-T Support 1 = 10BASE-T Half-Duplex is supported by the link partner 0 = 10BASE-T Half-Duplex is not supported by the link partner
5.4:5.0	Selector	<00000>,RO	Protocol Selection Bits Link partner's binary encoded protocol selector

8.7 Auto-Negotiation Expansion Register (ANER) – 06

Bit	Bit Name	Default	Description
6.15:6.5	RESERVED	0,RO	Reserved Read as 0, ignore on write
6.4	PDF	0,RO/LH	Local Device Parallel Detection Fault 1 = PDF: A fault detected via parallel detection function. 0 = PDF: No fault detected via parallel detection function
6.3	LP_NP_ABLE	0,RO	Link Partner Next Page Able 1 = LP_NP_ABLE: Link partner, next page available 0 = LP_NP_ABLE: Link partner, no next page
6.2	NP_ABLE	0,RO/P	Local Device Next Page Able 1 = NP_ABLE: DM9163, next page available 0 = NP_ABLE: DM9163, no next page DM9163 does not support this function, so this bit is always 0
6.1	PAGE_RX	0,RO/LH	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management
6.0	LP_AN_ABLE	0,RO	Link Partner Auto-Negotiation Able A “1” in this bit indicates that the link partner supports Auto-Negotiation

8.8 DAVICOM Specified Configuration Register (DSCR) - 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	0,RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
16.14	BP_SCR	0,RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
16.13	BP_ALIGN	0,RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
16.12	BP_ADPOK	0,RW	Bypass ADPOK 1=Reserved 0=Normal operation
16.11	REPEATER	RW	Repeater/Node Mode The value of the Repeater/Node is latched into this bit at power-up/reset 1 = Repeater mode 0 = Node mode *Please reference to 8.16 DAVICOM Hardware Reset Latch State Register (RLSR) – 24 (Bit 9)
16.10	TX	1,RW	100BASE-TX Mode Control 1 = 100BASE-TX operation
16.9	RESERVED	1,RO	Reserved
16.8	RMII_Enable	RW	Reduced MII Enable Select normal MII or RMII. The value of the RMII is latched into this bit at power-up/reset 1 = Enable RMII 0 = Normal MII *Please reference to 8.16 DAVICOM Hardware Reset Latch State Register (RLSR) – 24 (Bit 11)

16.7	F_LINK_100	0,RW	Force Good Link in 100Mbps 1 = Force 100Mbps good link status 0 = Normal 100Mbps operation This bit is useful for diagnostic purposes
16.6	SPLED_CTL	0,RW	Speed LED Disable 1 = Disable SPEED LED output. 0 = Normal SPEED LED output to indicate speed status
16.5	COLLED_CTL	0,RW	Collision LED Enable 1 = FDX/COL LED output is configured to indicate Full-Duplex/Collision status 0 = FDX/COL LED output is configured to indicate Full/Half-Duplex status
16.4	RPDCTR-EN	1,RW	Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 1 = Enable automatic reduced power down 0 = Disable automatic reduced power down
16.3	SMRST	0,RW	Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed
16.2	MFPSC	1,RW	MF Preamble Suppression Control MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0,RW	Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0,RW	Remote Loop out Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

8.9 DAVICOM Specified Configuration and Status Register (DSCSR) – 17

<table>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>17.15</td><td>100FDX</td><td>1,RO</td><td>100M Full-Duplex Operation Mode
After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Full-Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode</td></tr>
<tr><td>17.14</td><td>100HDX</td><td>1,RO</td><td>100M Half-Duplex Operation Mode
After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M Half-Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode</td></tr>
<tr><td>17.13</td><td>10FDX</td><td>1,RO</td><td>10M Full-Duplex Operation Mode
After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full-Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode</td></tr>
<tr><td>17.12</td><td>10HDX</td><td>1,RO</td><td>10M Half-Duplex Operation Mode
After Auto-Negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Half-Duplex mode. The software can read bit [15:12] to see which mode is selected after Auto-Negotiation. This bit is invalid when it is not in the Auto-Negotiation mode</td></tr>
<tr><td>17.11: 17.9</td><td>RESERVED</td><td>0,RO</td><td>Reserved
Read as 0, ignore on write</td></tr>
<tr><td>17.8 :17.4</td><td>PHYADR [4:0]</td><td>(PHYADR), RW</td><td>PHY Address Bit 4:0
The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY</td></tr>
<tr><td>17.3:17.0</td><td>ANMB[3:0]</td><td>0,RO</td><td>Auto-Negotiation Monitor Bits
These bits are for debug only. The Auto-Negotiation status will be written to these bits.
<table>
<tr><th>b3</th><th>b2</th><th>b1</th><th>B0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>In IDLE state</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Ability match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Acknowledge match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Acknowledge match fail</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Consistency match</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Consistency match fail</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Parallel detects signal_link_ready</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Parallel detects signal_link_ready fail</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Auto-Negotiation completed successfully</td></tr>
</table></td></tr>
</table>

8.10 10BASE-T Configuration/Status (10BTCSR) – 18

Bit	Bit Name	Default	Description
18.15	RESERVED	0,RO	Reserved Read as 0, ignore on write
18.14	LP_EN	1,RW	Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation
18.13	HBE	1,RW	Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the DM9163 is configured for Full-Duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in Full-Duplex mode)
18.12	SQUELCH	1,RW	Squelch Enable 1 = Normal squelch 0 = Low squelch
18.11	JABEN	1,RW	Jabber Enable Enables or disables the Jabber function when the DM9163 is in 10BASE-T Full-Duplex or 10BASE-T transceiver Loopback mode 1 = Jabber function enabled 0 = Jabber function disabled

18.10	10BT_SER	RW	10BASE-T GPSI Mode (Default value depend on #pin34 strap condition)
			1 = 10BASE-T GPSI mode selected (#pin34 pull down)
			0 = 10BASE-T MII mode selected (#pin34 pull up, default)
			GPSI mode is not supported for 100Mbps operation
			*Please reference to 8.16 DAVICOM Hardware Reset Latch State Register (RLSR) – 24 (Bit 10)

18.9:18.1	RESERVED	0,RO	Reserved Read as 0, ignore on write
18.0	POLR	0,RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is automatically set and cleared by 10BASE-T module

8.11 Power down Control Register (PWDOR) – 19

Bit	Bit Name	Default	Description
19.15:19.9	RESERVED	0,RO	Reserved Read as 0, ignore on write
19.8	PD10DRV	0,RW	Vendor power down control test
19.7	PD100DL	0,RW	Vendor power down control test
19.6	PDchip	0,RW	Vendor power down control test
19.5	PDcom	0,RW	Vendor power down control test
19.4	PDaeq	0,RW	Vendor power down control test
19.3	PDdrv	0,RW	Vendor power down control test
19.2	PDedi	0,RW	Vendor power down control test
19.1	PDedo	0,RW	Vendor power down control test
19.0	PD10	0,RW	Vendor power down control test

***** When selected, the power down value is control by Register 20.0

8.12 (Specified Config) Register – 20

Bit	Bit Name	Default	Description
20.15	TSTSE1	0,RW	Vendor test select control
20.14	TSTSE2	0,RW	Vendor test select control
20.13	RESERVED	0, RO	Reserved 0 = Normal SD
20.12	TSTSEL3	0,RW	Vendor test select control
20.11	PREAMBLEX	0,RW	Preamble Saving Control 1 = 10M TX preamble bit count is normal. 0 = When bit 10 is set, the 10M TX preamble count is reduced. When bit 11 of register 29 is set, 12-bit preamble bit is reduced. Otherwise 22-bit preamble bit is reduced
20.10	TX10M_PWR	0,RW	10M TX Power Saving Control 1 = Enable 10M TX power saving 0 = Disable 10M TX power saving
20.9	NWAY_PWR	0,RW	N-Way Power Saving Control 1 = Disable N-Way power saving 0 =Enable N-Way power saving
20.8	RESERVED	0,RO	Reserved Read as 0, ignore on write
20.7	MDIX_CNTL	MDI/MDIX,RO	The polarity of MDI/MDIX value 1 = MDIX mode 0 = MDI mode
20.6	AutoNeg_dpbk	0,RW	Auto-Negotiation Loopback 1 = Test internal digital Auto-Negotiation Loopback 0 = Normal.
20.5	Mdix_fix Value	0,RW	MDIX_CNTL force value: When MDIX_DOWN = 1, MDIX_CNTL value depend on the register value.
20.4	Mdix_do wn	0,RW	MDIX Down Manual force MDI/MDIX. 1 = Disable HP Auto-MDIX , MDIX_CNTL value depend on 20.5 0 = Enable HP Auto-MDIX
20.3	MonSel1	0,RW	Vendor monitor select
20.2	MonSel0	0,RW	Vendor monitor select
20.1	RMII_Ver	0,RW	RMII version 1 = Support RMII 1.0 0 = Support RMII 1.2
20.0	PD_value	0,RW	Power down control value Decision the value of each field Register 19. 1 = Power down 0 = Normal

8.13 DAVICOM Specified Interrupt Register – 21

Bit	Bit Name	Default	Description
21.15	INTR PEND	0,RO	Interrupt Pending Indicates that the interrupt is pending and is cleared by the current read. This bit shows the same result as bit 0. (INTR Status)
21.14: 21.12	RESERVED	0,RO	Reserved
21.11	FDX mask	1,RW	Full-Duplex Interrupt Mask When this bit is set, the Duplex status change will not generate the interrupt
21.10	SPD mask	1,RW	Speed Interrupt Mask When this bit is set, the Speed status change will not generate the interrupt
21.9	LINK mask	1,RW	Link Interrupt Mask When this bit is set, the link status change will not generate the interrupt
21.8	INTR mask	1,RW	Master Interrupt Mask When this bit is set, no interrupts will be generated under any condition
21.7:21.5	RESERVED	0,RO	Reserved
21.4	FDX change	0,RO/LH	Duplex Status Change Interrupt “1” indicates a change of duplex since last register read. A read of this register will clear this bit
21.3	SPD change	0,RO/LH	Speed Status Change Interrupt “1” indicates a change of speed since last register read. A read of this register will clear this bit
21.2	LINK change	0,RO/LH	Link Status Change Interrupt “1” indicates a change of link since last register read. A read of this register will clear this bit
21.1	RESERVED	0,RO	Reserved
21.0	INTR status	0,RO/LH	Interrupt Status The status of MDINTR#. “1” indicates that the interrupt mask is off that one or more of the change bits are set. A read of this register will clear this bit

8.14 DAVICOM Specified Receive Error Counter Register (RECR) – 22

Bit	Bit Name	Default	Description
22.15:0	Rcv_ Err_ Cnt	0,RO	Receive Error Counter Receive error counter that increments upon detection of RXER. Clean by read this register.

8.15 DAVICOM Specified Disconnect Counter Register (DISCR) – 23

Bit	Bit Name	Default	Description
23.15: 23.8	RESERVED	0,RO	Reserved
23.7:23.0	Disconnect Counter	0,RO	Disconnect Counter those increments upon detection of disconnection. Clean by read this register.

8.16 DAVICOM Hardware Reset Latch State Register (RLSR) – 24

Bit	Bit Name	Default	Description
24.15	LH_LEDMODE	1,RO	LEDMODE pin value
24.14	LH_MDINTR	1,RO	MDINTR pin reset latch value
24.13	LH_CSTS	0,RO	CABLESTS pin reset latch value (linksts)
24.12	LH_ISO	0,RW	TXCLK pin reset latch value (clk50m)
24.11	LH_RMII	0,RW	COL pin reset latch value (rmii)
24.10	LH_TP10SER	1,RW	RXCLK pin reset latch value (scamen)
24.9	LH_REPTR	0,RW	RXER pin reset latch value (repeater)
24.8	LH_TSTMOD	0,RW	RXDV pin reset latch value (speedup)
24.7	LH_OP2	1,RO	LNKLED pin reset latch value (opmode2)
24.6	LH_OP1	1,RO	SPDLED pin reset latch value (opmode1)
24.5	LH_OP0	1,RO	FDXLED pin reset latch value (opmode0)
24.4	LH_PH4	0,RO	CRS pin reset latch value (phy_addr4)
24.3	LH_PH3	0,RO	RXD3 pin reset latch value (phy_addr3)
24.2	LH_PH2	0,RO	RXD2 pin reset latch value (phy_addr2)
24.1	LH_PH1	0,RO	RXD1 pin reset latch value (phy_addr1)
24.0	LH_PH0	0,RO	RXD0 pin reset latch value (phy_addr0)

Note: Write Reg. 0x8000 into Reg. 0x00 after reset R/W value to make functions work.

8.17 Cable Control Register (CABCR) – 28

Bit	Bit Name	Default	Description
28.15:14	RESERVED	0,RO	Reserved
28.13	INV_50M	0,RW	50MHz clock output timing inverse
28.12	DLY_50M	0,RW	50MHz clock output delay 5ns
28.11	RESERVED	0,RO	Reserved
28.10:5	RESERVED	0,RW	Reserved
28.4:2	RESERVED	0,RO	Reserved
28.1:0	CABLE_CTRL	11,RW	Cable Control Threshold for receive cable status

8.18 Power Saving Control Register (PSCR) – 29

Bit	Name	Default	Description
29.15	BIST_start	0,RW	Start BIST test 1 = BIST start 0 = BIST stop
29.14	BIST_status	0,RO	BIST test status 1 = BIST pass. 0 = BIST fail. Latched, cleared when BIST is stopped.
29.13	BIST_i_loop	0,RW	Internal BIST 1 = Internal loop back 0 = External loop back
29.12	RESERVED	0,RO	Reserved
29.11	PREAMBLEX	0,RW	Preamble Saving Control When bit 10 of register 20 is set and bit 11 of register 20 is cleared, the 10M TX preamble count is reduced. 1 = 10-bit preamble bit is reduced. 0 = 20-bit preamble bits is reduced.
29.10	RESERVED	0,RO	Reserved
29.9	TX_PWR	0.RW	TX Power Saving Control Disabled 1 = Disable TX driving power saving function 0 = When cable is unconnected with link partner, the driving current of transmit is reduced for power saving.
29.8:0	RESERVED	0,RO	Reserved

9 DC and AC Electrical Characteristics

9.1 Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD	Supply Voltage	-0.3	3.6	V	*1
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	*2
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	*2
T_{STG}	Storage Temperature range	-65	+150	°C	-
TA	Ambient Temperature	-40	+85	°C	
LT	Lead Temperature (L_T, soldering, 10 sec.).	-	+260	°C	-

*1: Power pin
*2: IO pin

9.2 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DVDD	Supply Voltage	3.135	3.300	3.465	V	
PD (Power Dissipation) *	100BASE-TX	-	130	-	mA	3.3V
	10BASE-T	-	120	-	mA	3.3V
	Auto-Negotiation	-	50	-	mA	3.3V
	Power Down Mode	-	8.2	-	mA	3.3V

Comments
Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated that in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.3 DC Electrical Characteristics (DVDD = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IL}	Input Low Voltage	-	-	0.8	V	All Design Pin Except RESET#,DISMDIX
V_{IH}	Input High Voltage	2.0	-	-	V	All Design Pin Except RESET#,DISMDIX
V_{ILs}	Schmitt Trigger Input Low Threshold Voltage	-	0.9	1.0	V	For RESET#,DISMDIX
V_{IHs}	Schmitt Trigger Input High Threshold Voltage	1.45	1.55	-	V	For RESET#,DISMDIX
I_{IL}	Input Low Leakage Current	-1	-	-	uA	V_{IN} = 0V
I_{IH}	Input High Leakage Current	-	-	1	uA	V_{IN} = 3.3V
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL} = 4mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH} = -4mA
Receiver						
V_{ICM}	RX+/RX- Common mode Input Voltage	-	3.3	-	V	100 Ω Termination Across
Transmitter						
$V_{TD}100$	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
$V_{TD}10$	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
$I_{TD}100$	100TX+/- Differential Output Current	19	20	21	mA	
$I_{TD}10$	10TX+/- Differential Output Current	44	50	56	mA	

9.4 AC Electrical Characteristics & Timing Waveforms

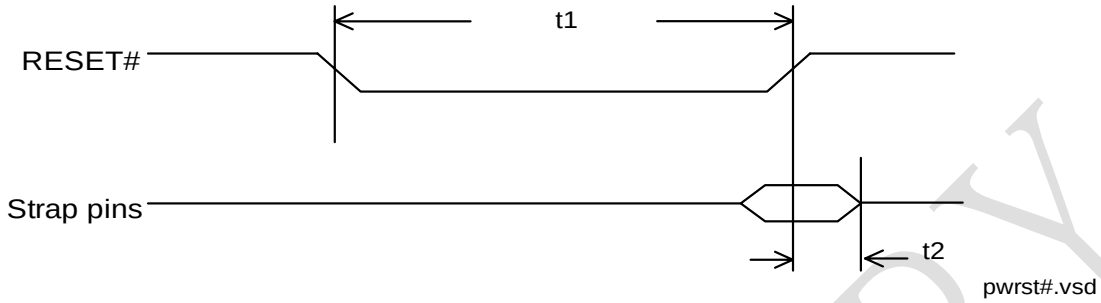
9.4.1 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
t_{TM}	100TX+/- Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
t_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
t_{TJT}	100TX+/- Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
X_{OST}	100TX+/- Differential Voltage Overshoot	0	-	5	%	

9.4.2 Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	OSC Frequency	24.99925	25	25.00075	MHz	30ppm
t_{CKC}	OSC Cycle Time	39.9988	40	40.0012	ns	30ppm
t_{PWH}	OSC Pulse Width High	16	20	24	ns	
t_{PWL}	OSC Pulse Width Low	16	20	24	ns	

9.4.3 Power On Reset Timing

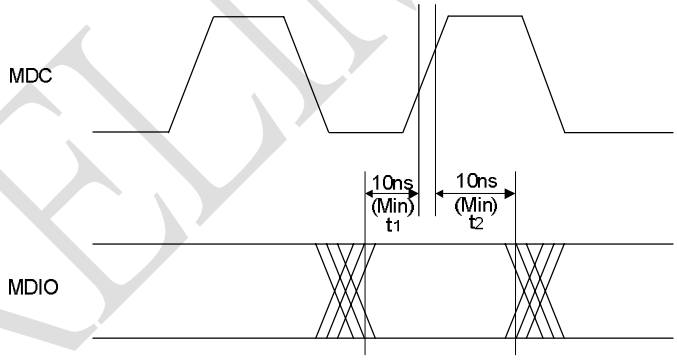


Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	RESET# Low Period	1	-	-	ms	-
t2	Strap pin hold time with RESET#	40	-	-	ns	-

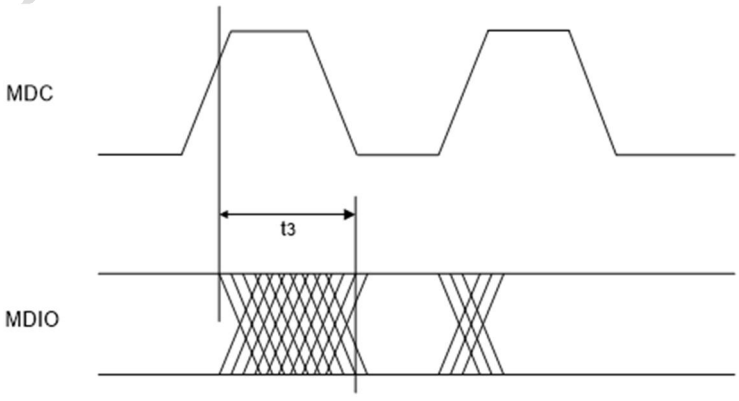
9.4.4 MDC/MDIO Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t0	MDC Cycle Time	400	-	-	ns	
t1	MDIO Setup Before MDC	10	-	-	ns	When OUTPUT By STA
t2	MDIO Hold After MDC	10	-	-	ns	When OUTPUT By STA
t3	MDC To MDIO Output Delay	2	-	-	ns	When OUTPUT By DM9163

9.4.5 MDIO Timing When OUTPUT by STA



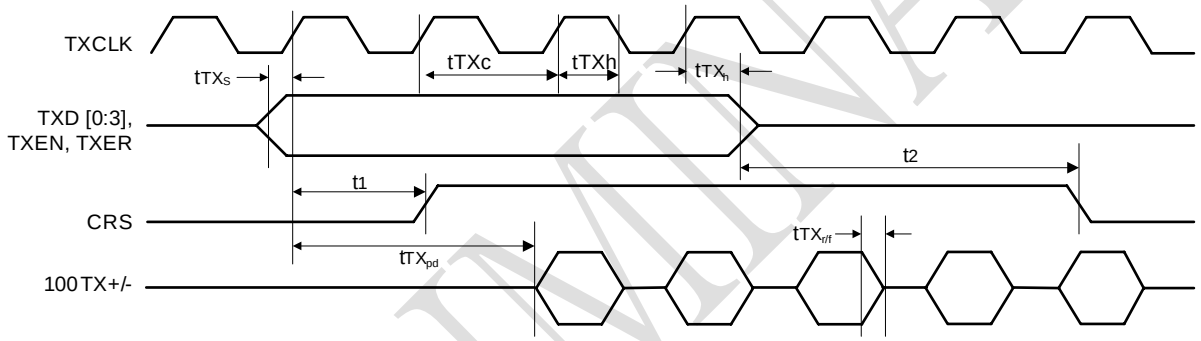
9.4.6 MDIO Timing When OUTPUT by DM9163



9.4.7 MII 100BASE-TX Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{TXc}	TXCLK Cycle Time	39.9988	40	40.0012	ns	30ppm
t_{TXh}, t_{TXl}	TXCLK High/Low Time	16	20	24	ns	
t_{TX_s}	TXD [0:3], TXEN, TXER Setup To TXCLK High	12	-	-	ns	
t_{TX_h}	TXD [0:3], TXEN, TXER Hold From TXCLK High	0	-	-	ns	
t_1	TXEN Sampled To CRS Asserted	-	4	-	BT	
t_2	TXEN Sampled To CRS De-asserted	-	4	-	BT	
$t_{TX_{pd}}$	TXEN Sampled To TX+/- Out (Tx Latency)	-	8	-	BT	
$t_{TX_{r/f}}$	100TX Driver Rise/Fall Time	3	4	5	ns	90% To 10%, Into 100ohm Differential
Note 1. Typical values are at 25℃and are for design aid only; not guaranteed and not subject to production testing.						

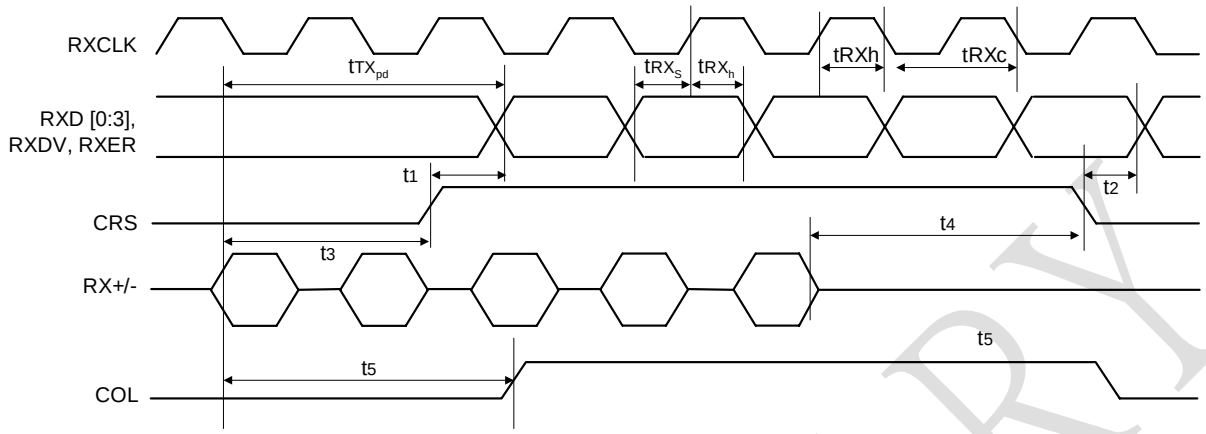
9.4.8 MII 100BASE-TX Transmit Timing Diagram



9.4.9 MII 100BASE-TX Receive Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RXc}	RXCLK Cycle Time	39.9988	40	40.0012		30ppm
T_{RXh}, t_{RXl}	RXCLK High/Low Time	16	20	24		
t_{RX_s}	RXD [0:3], RXDV, RXER Setup To RXCLK High	10	-	-	ns	
t_{RX_h}	RXD [0:3], RXDV, RXER Hold From RXCLK High	10	-	-	ns	
$t_{RX_{pd}}$	RX+/- In To RXD [0:3] Out (Rx Latency)	-	15	-	BT	
t_1	CRS Asserted To RXD [0:3], RXDV, RXER	-	4	-	BT	
t_2	CRS De-asserted To RXD [0:3], RXDV, RXER	-	0	-	BT	
t_3	RX+/- In To CRS Asserted	10	-	14	BT	
t_4	RX+/- Quiet To CRS De-asserted	14	-	18	BT	
t_5	RX+/- In To COL De-Asserted	14	-	18	BT	
1. Typical values are at 25℃and are for design aid only; not guaranteed and not subject to production testing.						

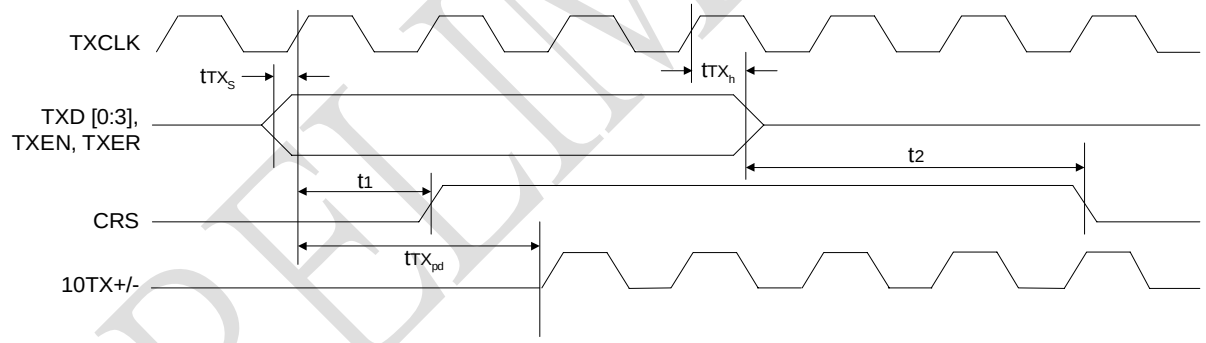
9.4.10 MII 100BASE-TX Receive Timing Diagram



9.4.11 MII 10BASE-T Nibble Transmit Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTX_S	TXD[0:3), TXEN, TXER Setup To TXCLK High	5	-	-	ns	
tTX_h	TXD[0:3], TXEN, TXER Hold From TXCLK High	5	-	-	ns	
t1	TXEN Sampled To CRS Asserted	-	2	4	BT	
t2	TXEN Sampled To CRS De-asserted	-	15	20	BT	
tTX_{pd}	TXEN Sampled To 10TX+/- Out (Tx Latency)	-	2	4	BT	

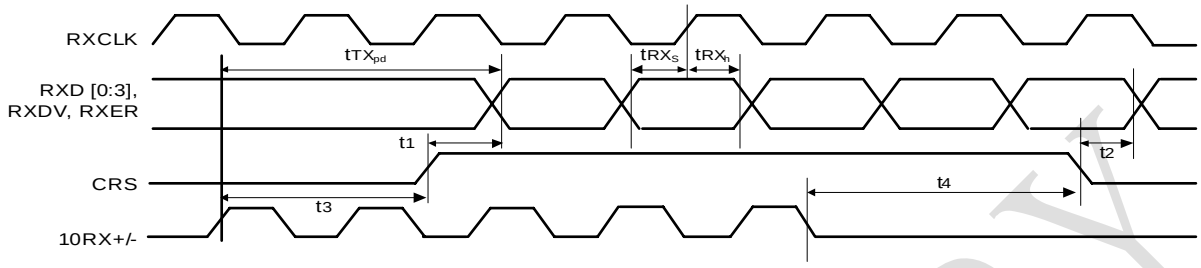
9.4.12 MII 10BASE-T Nibble Transmit Timing Diagram



9.4.13 MII 10BASE-T Receive Nibble Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRX_S	RXD [0:3], RXDV, RXER Setup To RXCLK High	5	-	-	ns	
tRX_h	RXD [0:3], RXDV, RXER Hold From RXCLK High	5	-	-	ns	
tRX_{pd}	10RX+/- To RXD [0:3] Out (Rx Latency)	-	7	-	BT	
t1	CRS Asserted To RXD [0:3], RXDV, RXER,Asserted	1	14	20	BT	
t2	CRS De-asserted To RXD [0:3], RXDV, RXER,De-asserted	-	-	3	BT	
t3	RXI In To CRS Asserted	1	2	4	BT	
t4	RXI Quiet To CRS De-asserted	1	10	15	BT	

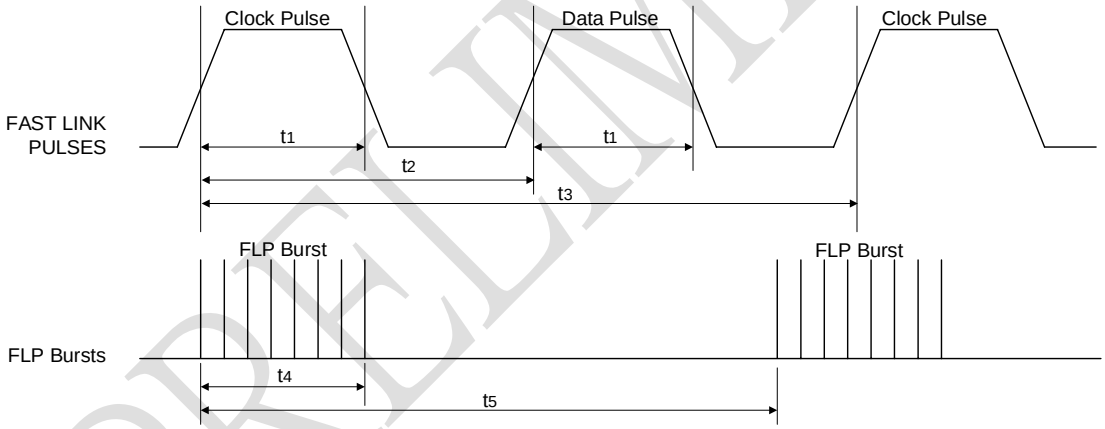
9.4.14 MII 10BASE-T Receive Nibble Timing Diagram



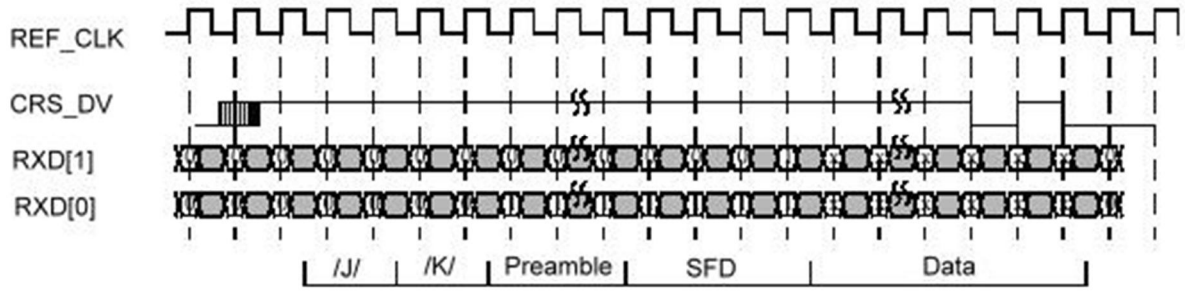
9.4.15 Auto-Negotiation and Fast Link Pulse Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t1	Clock/Data Pulse Width	-	100	-	ns	
t2	Clock Pulse To Data Pulse Period	55.5	62.5	69.5	us	DATA = 1
t3	Clock Pulse To Clock Pulse Period	111	125	139	us	
t4	FLP Burst Width	-	2	-	ms	
t5	FLP Burst To FLP Burst Period	8	-	24	ms	
-	Clock/Data Pulses in a Burst	17	-	33	pulse	

9.4.16 Auto-Negotiation and Fast Link Pulse Timing Diagram

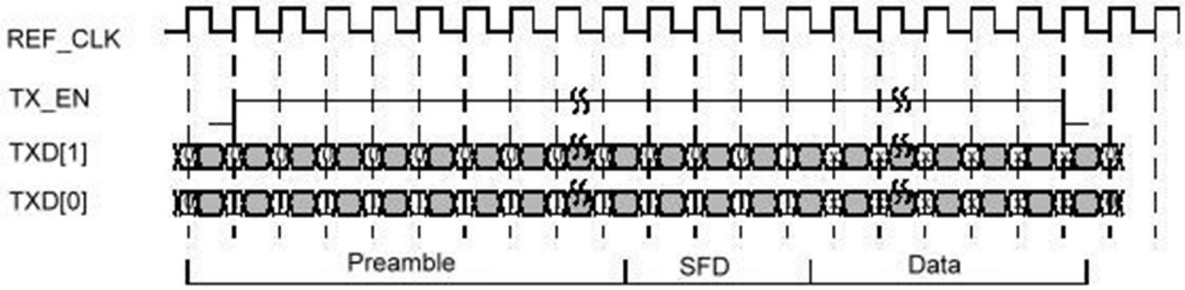


9.4.17 RMII Receive Timing Diagram



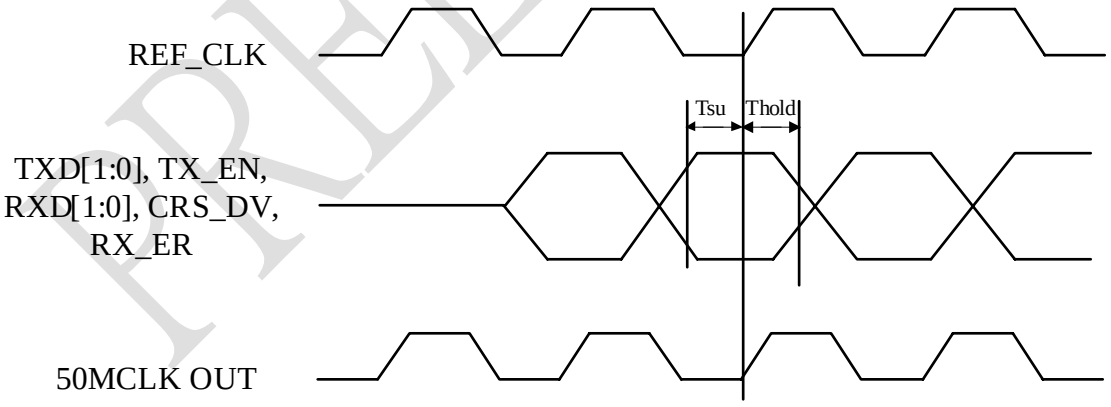
100 Mb/s Reception with no errors

9.4.18 RMII Transmit Timing Diagram



100 Mb/s Transmission

9.4.19 RMII Timing Diagram



9.4.20 RMII Timing Parameter

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Fref	REF_CLK Frequency (External clock source)	49.9985	50	50.0015	MHz	30ppm (1.5KHz)
50MCLK OUT	50Mhz_CLK Output Frequency (DM9163 output clock)	49.9985	50	50.0015	MHz	30ppm (1.5KHz)
Tref%	REF_CLK Duty Cycle	35	-	65	%	
Tref	REF_CLK Clock Cycle		20	-	ns	30ppm
Tsu	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge	4	-	-	ns	
Thold	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER Data hold from REF_CLK rising edge	2	-	-	ns	

9.4.21 Magnetic Selection Guide

Refer to Table 2 for transformer requirements. Transformers, meeting these requirements, are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic before using them in an application. The transformers listed in Table 2 are electrical equivalents, but may not be pin-to-pin equivalents.

Refer to the following tables 5-1 and 5-2 for 10/100M magnetic sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
MAGCOM	HS9016, HS9024
Delta	LFE8563-DC, LFE8563T-DC

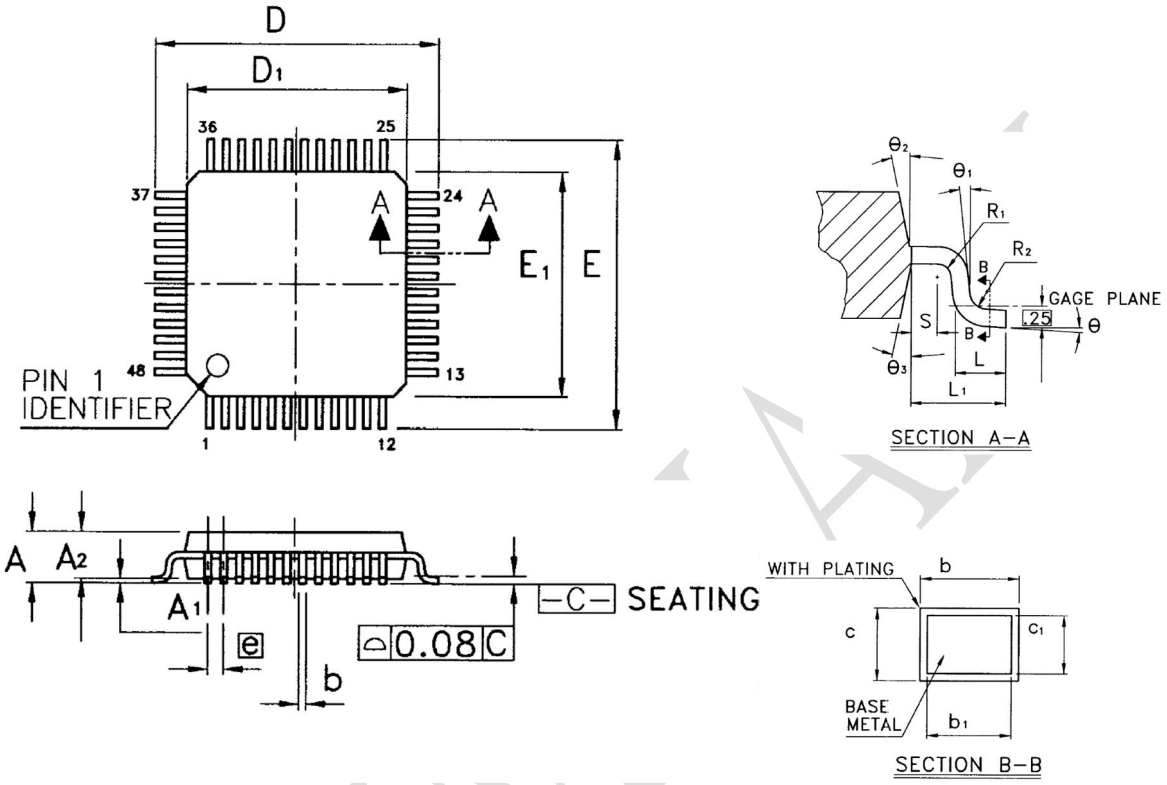
Table 5-1: 10/100M Magnetics Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	µH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 –30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 5-2: Magnetic Specification Requirements

10 Package Information

48 Pins LQFP Package Outline Information:



Symbol	Dimension in mm				Dimension in inch		
	Min	Nom	Max		Min	Nom	Max
A	–	–	1.60		–	–	0.063
A_1	0.05	–	0.15		0.002	–	0.006
A_2	1.35	1.40	1.45		0.053	0.055	0.057
b	0.17	0.22	0.27		0.007	0.009	0.011
b_1	0.17	0.20	0.23		0.007	0.008	0.009
c	0.09	–	0.20		0.004	–	0.008
c_1	0.09	–	0.16		0.004	–	0.006
D	9.00 BSC				0.354 BSC		
D_1	7.00 BSC				0.276 BSC		
E	9.00 BSC				0.354 BSC		
E_1	7.00 BSC				0.276 BSC		
e	0.50 BSC				0.020 BSC		
L	0.45	0.60	0.75		0.018	0.024	0.030
L_1	1.00 REF				0.039 REF		
R_1	0.08	–	–		0.003	–	–
R_2	0.08	–	0.20		0.003	–	0.008
S	0.20	–	–		0.008	–	–
θ	0^o	3.5^o	7^o		0^o	3.5^o	7^o
θ_1	0^o	–	–		0^o	–	–
θ_2	12^o TYP				12^o TYP		
θ_3	12^o TYP				12^o TYP		

1. Dimension D_1 and E_1 do not include resin fin.
2. All dimensions are base on metric system.
3. General appearance spec should base on its final visual inspection spec.

11 Ordering Information

Part Number	Pin Count	Package
DM9163EP	48	LQFP(Pb-Free)

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Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.