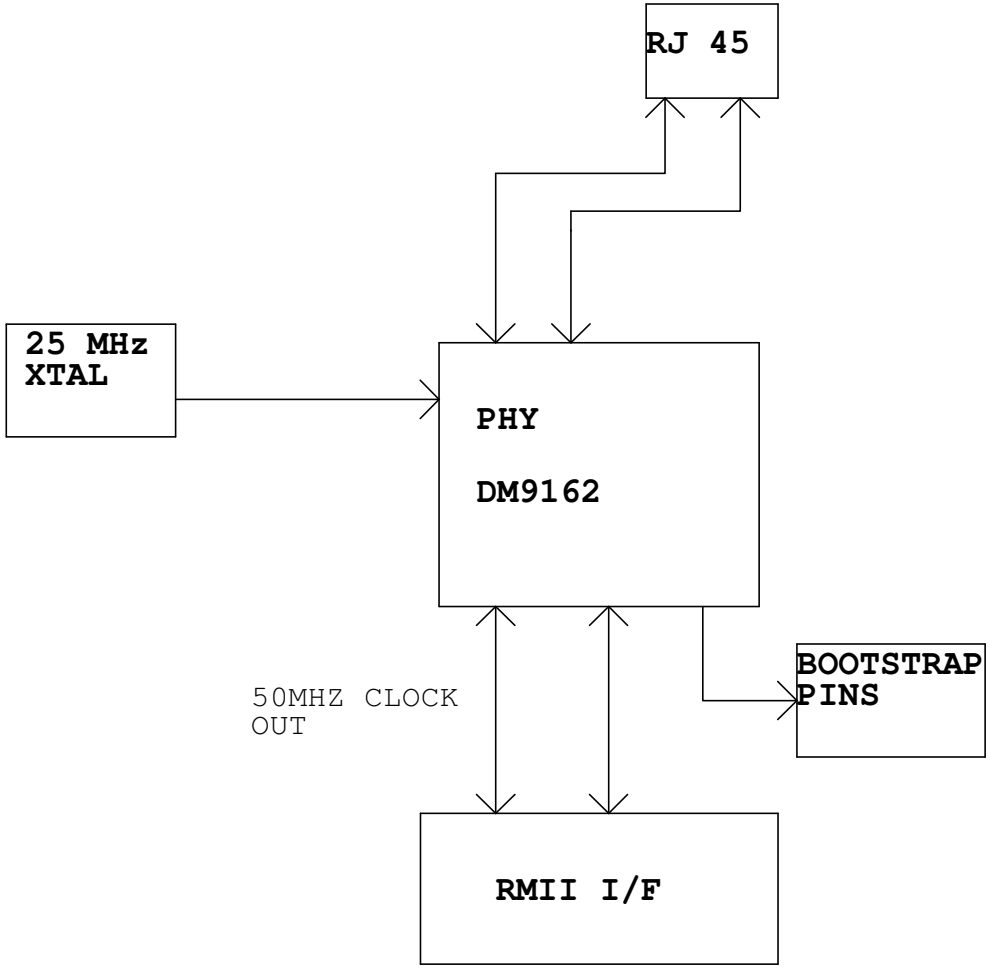

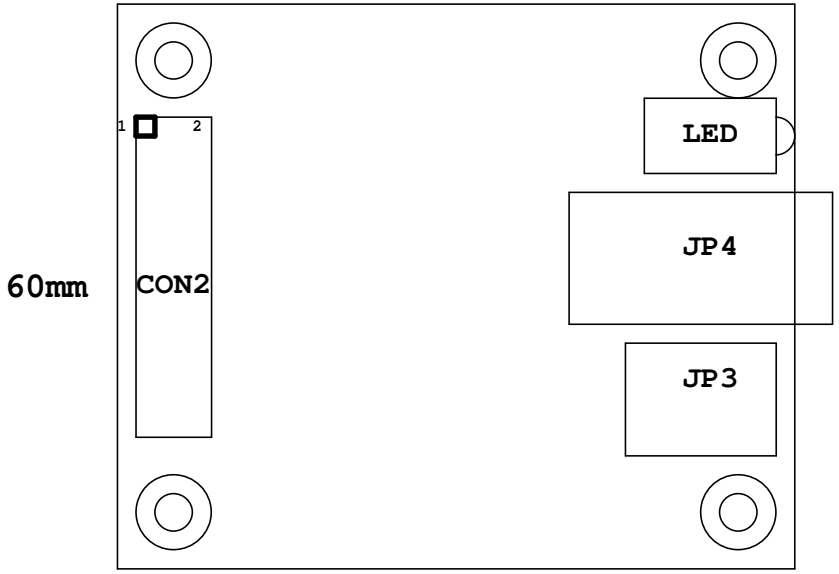

POWER FROM MII
+5V IN
+3.3V OUT
POWER
+3.3V IN
+1.8V OUT

Davicom Semiconductor Inc.		
Title: PHY Demo Board (PCB_Overview)		
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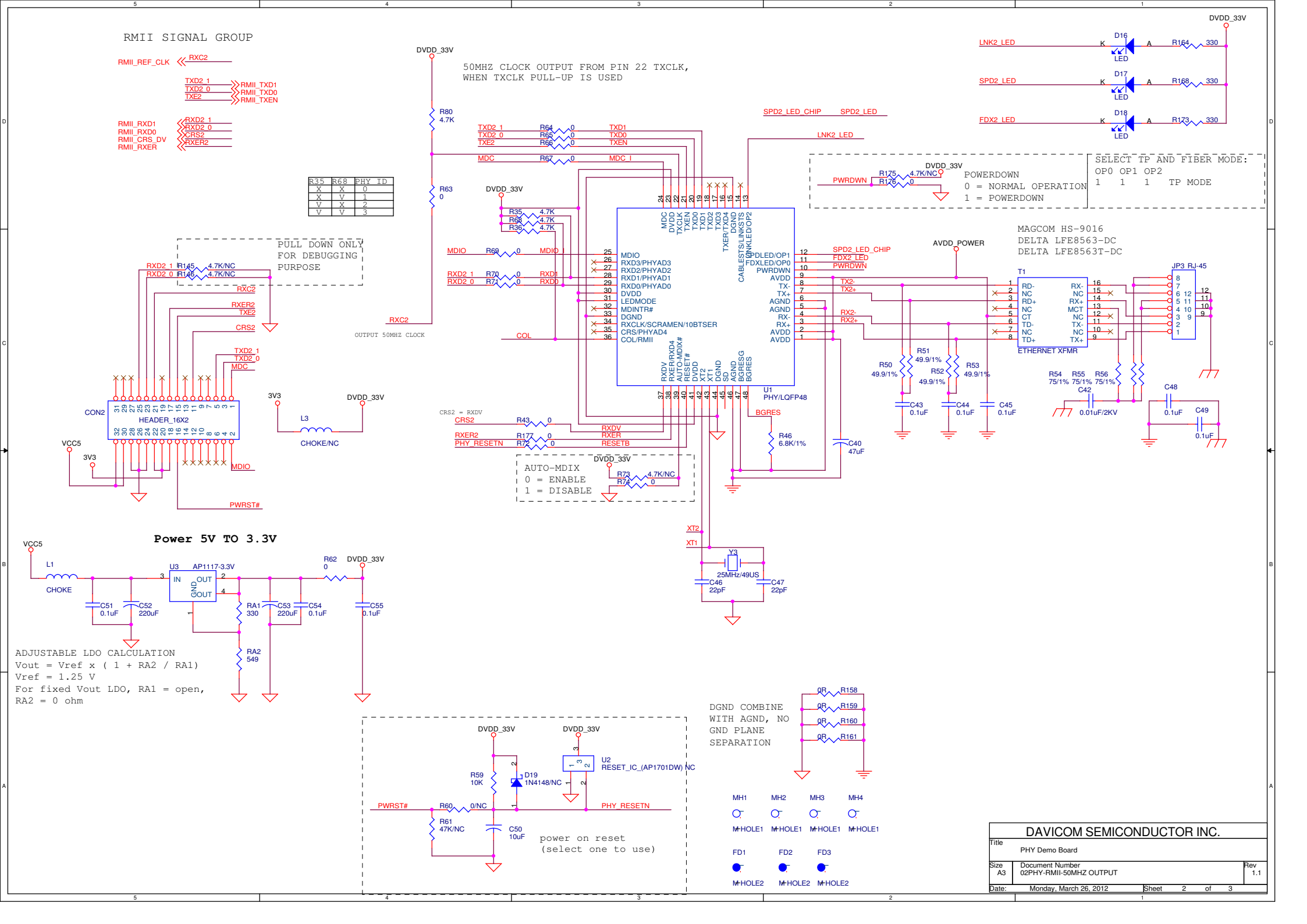
RMII SIGNAL GROUP
RMII_REF_CLK
RXC2
TXD2_1
TXD2_0
TXE2
RMII_TXD1
RMII_TXD0
RMII_TXEN
RMII_RXD1
RMII_RXD0
RMII_CRS_DV
RMII_RXER
RXD2_1
RXD2_0
CRS2
RXER2
R35 R68 PHY ID
X X 0
X V 1
V X 2
V V 3
DVDD_33V
50MHZ CLOCK OUTPUT FROM PIN 22 TXCLK,
WHEN TXCLK PULL-UP IS USED
R80 4.7K
R63 0
R64 0
R65 0
R66 0
R67 0
TXD1
TXD0
TXEN
MDC
MDC_I
R35 4.7K
R68 4.7K
R36 4.7K
MDIO
R69 0
MDIO_I
R70 0
R71 0
RXD1
RXD0
RXC2
OUTPUT 50MHZ CLOCK
COL
CRS2 = RXDV
CRS2
R43 0
RXER2
R177 0
PHY_RESETN
R72 0
RXDV
RXER
RESETB
U1
PHY/LQFP48
MDIO
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
DVDD
LEDMODE
MDINTR#
DGND
RXCLK/SCRAMEN/10BTSER
CRS/PHYAD4
COL/RMII
RXDV
RXER/RXD4
AUTO-MDIX#
RESET#
XT2
XT1
SD
AGND
BGRESG
BGRES
CABLESTS/LINKSTS
DNKLEDOP2
SPDLED/OP1
FDXLED/OP0
PWRDWN
AVDD
TX-
TX+
RX-
RX+
SPD2_LED_CHIP
SPD2_LED
LNK2_LED
FDX2_LED
PWRDWN
R175 4.7K/NC
R176 0
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
D16 LED
D17 LED
D18 LED
R164 330
R168 330
R173 330
LNK2_LED
SPD2_LED
FDX2_LED
PULL DOWN ONLY
FOR DEBUGGING
PURPOSE
R145 4.7K/NC
R146 4.7K/NC
CON2
HEADER_16X2
VCC5
3V3
MDIO
PWRST#
L3
CHOKE/NC
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC
R74 0
AVDD_POWER
MAGCOM HS-9016
DELTA LFE8563-DC
DELTA LFE8563T-DC
T1
RD-
NC
RD+
NC
CT
TD-
NC
TD+
RX-
NC
RX+
MCT
NC
TX-
NC
TX+
ETHERNET XFMR
JP3 RJ-45
TX2-
TX2+
RX2-
RX2+
R50 49.9/1%
R51 49.9/1%
R52 49.9/1%
R53 49.9/1%
R54 75/1%
R55 75/1%
R56 75/1%
C42 0.01uF/2KV
C43 0.1uF
C44 0.1uF
C45 0.1uF
C48 0.1uF
C49 0.1uF
R46 6.8K/1%
C40 47uF
XT2
XT1
Y3
25MHz/49US
C46 22pF
C47 22pF
Power 5V TO 3.3V
VCC5
L1
CHOKE
U3 AP1117-3.3V
IN
OUT
GND
GOUT
C51 0.1uF
C52 220uF
C53 220uF
C54 0.1uF
C55 0.1uF
R62 0
DVDD_33V
RA1 330
RA2 549
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open,
RA2 = 0 ohm
DVDD_33V
DVDD_33V
R59 10K
D19 1N4148/NC
U2 RESET_IC_(AP1701DW) NC
PWRST#
R60 0/NC
R61 47K/NC
C50 10uF
PHY_RESETN
power on reset
(select one to use)
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
0R R158
0R R159
0R R160
0R R161
MH1 MH2 MH3 MH4
M-HOLE1
FD1 FD2 FD3
M-HOLE2
DAVICOM SEMICONDUCTOR INC.
Title
PHY Demo Board
Size A3
Document Number
02PHY-RMII-50MHZ OUTPUT
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VER	DATE	ENGINEER	NOTE
1.0	12/12/2007	WILLIE NIOU	INITAL CIRCUIT CREATION
1.1	4/12/2010	WILLIE NIOU	BUG FIX AND ENHANCEMENTS: 1. CON2 GND CONNECT TO BOARD GND 2. LED LAYOUT LIBRARY NOT SAME AS ACUTAL COMPONENT USED. NEED TO CHANGE DIRECTION 180 DEGREES 3. C42 NEED TO CONNECT PIN 2 AND 3 TOGETHER 4. AGND AND DGND CONNECTED 5. ADD SPEED LED CONTROL CIRCUIT, DUE TO DM9161B DESIGN 6. ADD EXTERNAL 1.8V LDO FOR INPUT TO CENTER TAP OF TRANSFORMER TO REDUCE HEAT DISSIPATION BY CHIP
	2011/7/5	ALLIANG	1: ADD Fiber Module and termination circuit 2: CN2 MII Connector change to 16*2 Pinch 2.54mm 3: Change LED Anode & Cathode 4: Add R63,R80 For TXCLK and RXCLK wire link

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Title: PHY Demo Board (History)		
Size: A4	Document Number: HISTORY	Rev: 1.1
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