DAVICOM Semiconductor, Inc.

Layout Guide

Contents

1. Purpose

This document is used for Davicom customers as quickly reference to design PCB layout and to reduce ESD and EMI problem. Most topics are described in general case because the EMI and ESD problem are related to the total system, not only the Davicom chips but also others.

2. PCB stackups[1]

There are many kinds of PCB stack can be used. The simplest and general is 2 layers design but it is also the worst for high speed device.

Figure 1

Figure 1 shows the normal stack topology for 2 layers PCB design, due to this is hard to maintain the integrity of ground and power plane, the return current will be unpredictable in high speed circuit.

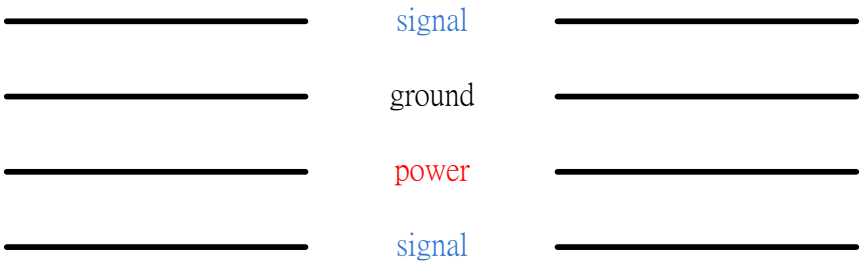


Figure 2

4 layers stack is presented in Figure 2. Between 2 signal layers, there is one ground and one power plane used to maintain the signal integrity. For return current, power plane is treated as the ground and provide it a well path to return to the source. If the ground and power plane are designed well, the return current will go back to source smoothly and this is the best strategy for EMI.

[1] Douglas Brooks, *Signal Integrity Issue and Printed Circuit Board Design* (Prentice Hall PTR, 2003).

Here is the Figure 3, shows the normal 6 layers stackup. Notice that there are 2 signal layers putted together; although, there are a ground and a power plane for each other's return current to go back, but for high speed data, the current will induce a magnetic field around its trace, the different magnetic fields will affect each other and result in the coupling.

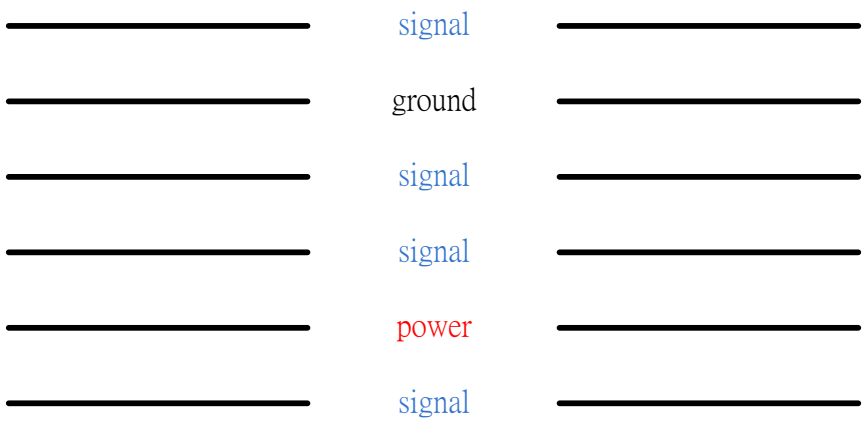


Figure 3

In order to reduce the coupling of signals, Figure 4 and 5 show two better ways for 6 layers PCB stackup.

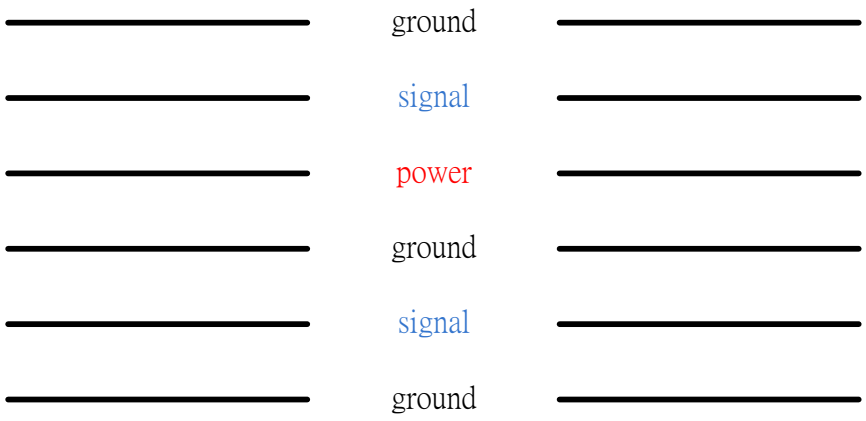


Figure 4

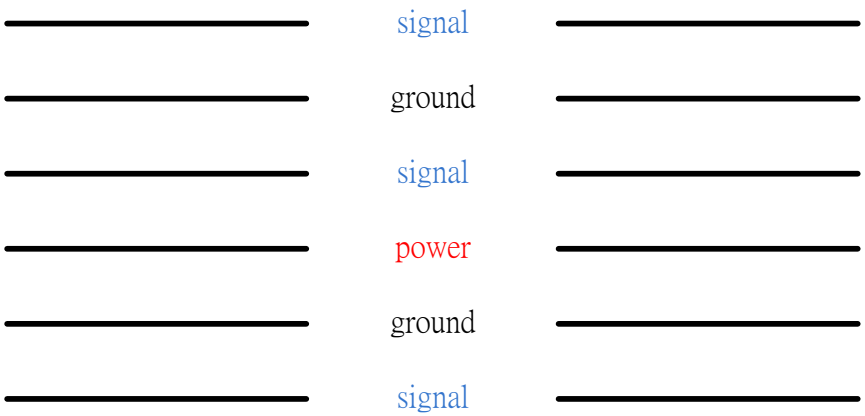


Figure 5

Figure 4 is the best way for PCB designer and also has the best EMI shielding performance because of 2 signal layers are buried in ground and power planes. There will be no EMI emits from signal traces. With the great advantage, here is one defect that the traces can't be too complicated because of there is only 2 signal layers for linking up every components.

Figure 5 can be adopted in the more complicated system because of there are 3 signal layers which increase the flexibility of the routing topology.

For Davicom products, at least 4 layers PCB stackup is recommended.

3. Power and ground plane strategy

There are several power requirements in most of today's systems. Different voltage levels, like 3.3V or 1.8V will be divided into different planes. Sometimes, the same voltage level will be also divided into several blocks and connected each other by inductor or bead for reducing of the noise.

Ground is normally divided in three parts in application, they are digital, analog and earth. Earth or chassis ground is used to be placed under the connector with metallic fingers. Some of the applications will place it at the edge around the PCB board with via to be an electrical fence to reduce fringing effect.

Different of Davicom products needs difference power planes; Table 1 shows the requirement of each others.

The ground planes for Davicom products are suggested to be divided into two parts, ground and earth. AGND and DGND are suggested to be combined for Davicom products, this will reduce the EMI. The connection of ground and earth will be shown in later topics.

For power plane, a pi filter with bead is suggested to be added from system 3.3V to Davicom products, like below figure 6.

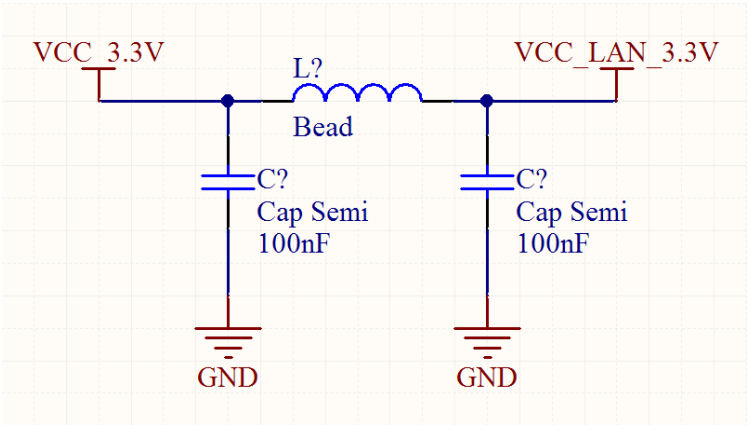


Figure 6

IC	3.3V	2.5V	1.8V
PHY			
DM9161	✓		
DM9161A	✓	✓	
DM9161B(BI)	✓		✓
NIC			
DM9000	✓		
DM9000A	✓	✓	
DM9000B(BI)	✓		✓
DM9008C	✓		✓
DM9010	✓	✓	
DM9010B	✓		✓
DM9102D	✓	✓	
DM9102H	✓		✓
DM9601	✓	✓	
DM9620	✓		✓
Switch			
DM8203/DM8206	✓		✓
DM9003/DM9006	✓		✓
DM9013/DM9016	✓		✓
DM9103/DM9106	✓		✓
DM9302/DM9332	✓		✓

Table 1

4. Overlapping of planes

Since power and ground will be separated to several parts according to their electrical characteristics. Figure 7 shows that a system with separated digital and analog of power and ground. It is obviously that there is an overlapping section of Digital VCC and Analog Ground; the noise will be easily coupled to each plane because the edge on the plane contains the strongest electrical field. In PCB design, this should be avoided.

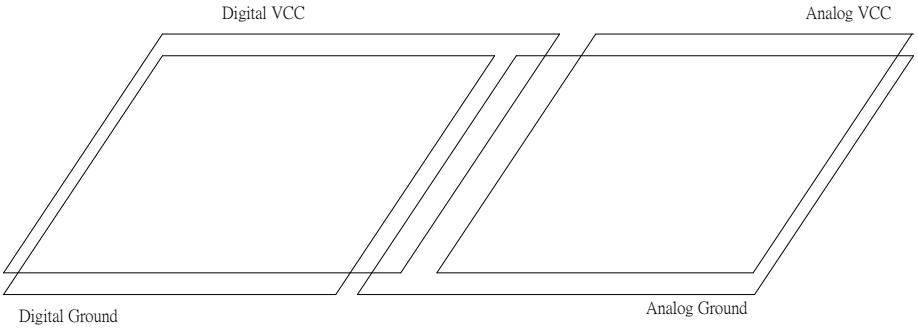


Figure 7

5. Data bus

The guard band of ground is used by in many cases to separate data bus traces by use pour or hash function to fill up the empty space of ground; it is a good idea but in some cases will induce more noise than without guard band.

Figure 8 shows a layout for PCI bus. The gray lines stand for data lines while the red color represents ground. It is obviously that some grounds were placed between traces with narrow width. This kind of placement will induce more noise if there is no well designed via to connect to inner ground plane.

It should be notice of this kind of problem, if the pour/hash function is enabled to fill the empty space with ground. Vias should be placed separately and randomly to reduce the coupling effect. Otherwise, it will result in data error problem, easily.

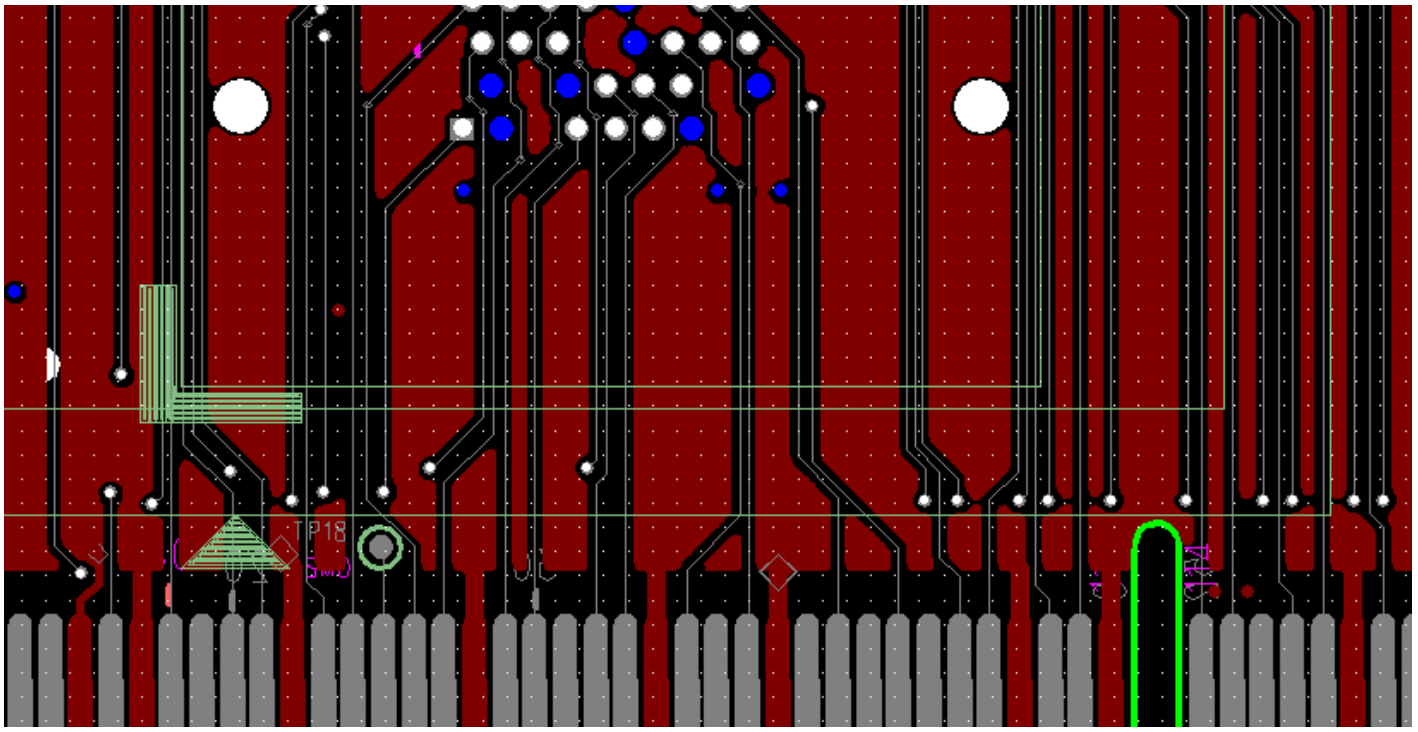


Figure 8

6. PCI data bus constrain[2]

The maximum trace length is 1.5 inches from the edge connector of expansion slot, except the group of system pins (CLK, RST#, AD[31::00], C/BE[3::0]#, and PAR), interrupt pins and JTAG pins.
The trace length for PCI CLK signal is 2.5 inches ± 0.1 inches.
The impedance should be controlled to be in the 60~100Ω. The trace velocity must be between 150 ps/inch and 190 ps/inch.

7. Media Independent Interface (MII)

There are 2 clock traces, TXCLK and RXCLK, exist on this kind of data bus. They are also the serious EMI sources in the system.
A microstrip line of characteristic impedance of 50Ω should be implement on each clock trace for reducing the reflection and keeping the signal integrity.
Another skill is putting series resistor next to the pin of PHY, the TXCLK and RXCLK is generated by PHY. In most case the resistance should equal to the characteristic impedance, 50Ω, to absorb the reflection waves.

8. Reduce Media Independent Interface (RMII)[3]

There is no TXCLK nor RXCLK exist on this bus, instead of them there is a 50MHz clock trace connects to PHY and MAC. With higher frequency, this trace should be treated carefully as a transmission line, also. Due to the clock trace will be divided into two parts; the layout should be carefully designed.
Figure 9 shows a typically design of this kind of application. There are some design constrains.

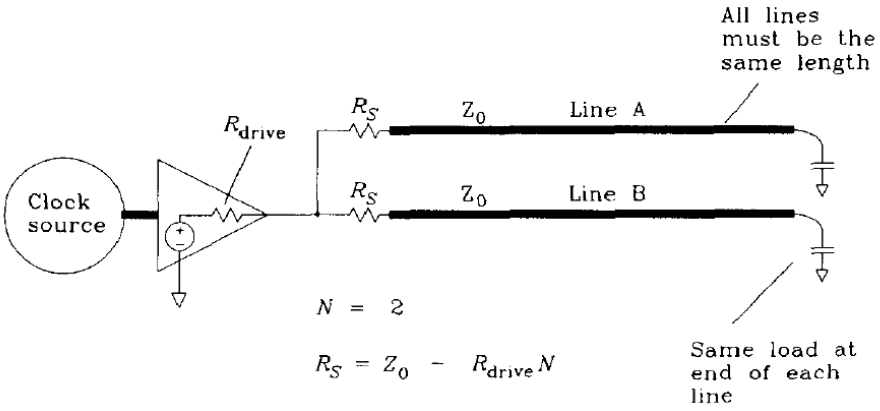


Figure 9

[2] *PCI Local Bus Specification Reversion 2.2* (PCI SIG, 1998)

[3] Johnson Graham, *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall PTR, 1993)

Multiple source termination with nonzero driver impedance works only if the lines are equally long and the loads at each end are balanced. The termination resistance must equal $R_S = Z_0 - R_{drive}N$, where R_S = source termination resistance, Z_0 = driven line impedance, R_{drive} = effective output impedance of driver and N = driven lines.
In RMII case, the $Z_0 = 50\ \Omega$, the R_S can be calculated easily by the formula above.

9. Crystal placement

Each Davicom IC needs at least one crystal or oscillator to work well. The placement of crystal, somehow, is important to reduce noise and EMI.
For crystal, it needs 2 traces to connect to Davicom IC; the suggestion is place it as close as possible. The capacitor placement is suggested below.

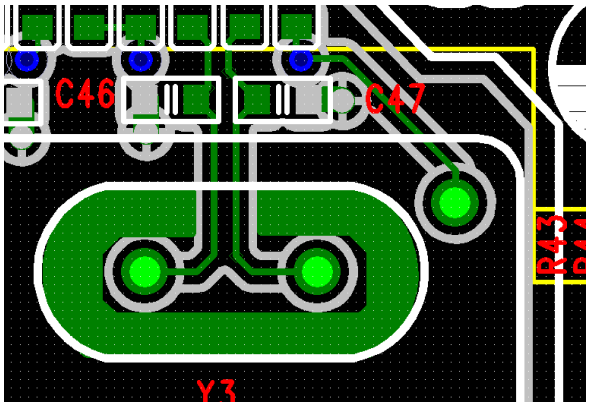
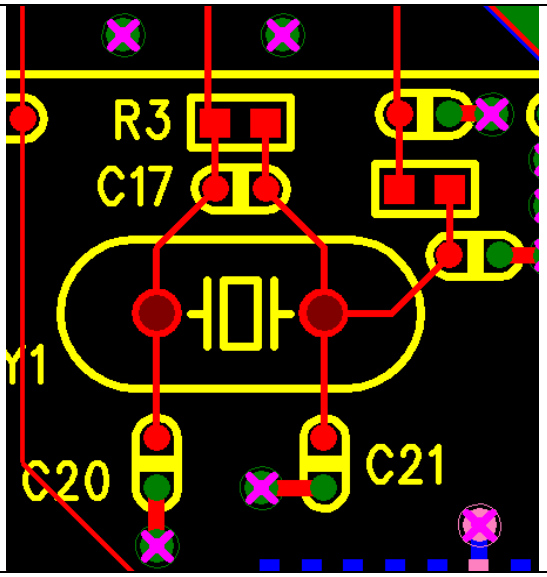
Better	Worse
	

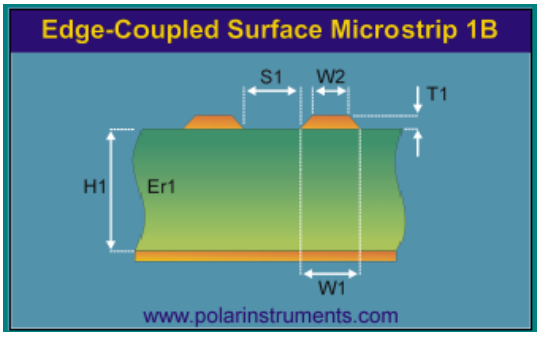
Table 2

Some PCB engineers will place the capacitors like the Worse one, it is obviously that the signal will travel into two directions, this is not good for signal integrity, the Better one is the suggested placement, because of there is only one direction.

10. Differential pairs between IC and transformer

It has at least 2 pairs of differential lines on every Davicom IC for communicating outside world. The signal exists on these lines are analogs.

The pair should be carefully designed to have differential characteristic impedance of 100Ω to reduce reflection. Most of the PCB manufacturer can help designer to accomplish this. Below is an example for you to reference. Table 3 is the parameters for assuming the PCB is assembled by 4 layers, FR4 material and 0.5 oz. copper. The calculation is done by Polar Si9000.



Field	Value
H1 (mm)	0.5333
Er1	4.4
W1 (mm)	0.4983
W2 (mm)	0.4729
S1 (mm)	0.2032
T1 (mm)	0.0178
Zdiff (Ω)	100

Table 3

The distance between 2 pairs should larger than 0.5 mm. It is better to have 1 mm separation distance.

The traces should be controlled as short as possible, too, the shorter the distance, the fewer the decay of signal amplitude and the better the signal integrity. Some of the applications will have a large distance between IC and RJ-45 connector, this kind of design should be avoid because the jitter will increase and the amplitude will decay with the increasing of the length. As what mentioned before, this kind of application should place transformer as near IC possible and leave the trace between connector and transformer long will be better.

11. Common mode choke placement

A common mode choke should be placed at the near end of the differential pair for reducing the common mode current which will inject to the PCB and raise the EMI value. The common mode choke value can be chosen to suit the system. The line can be shorted by 0 ohm also, if it is not the essential part after EMI test. Below figure shows the schematic for termination circuit, TVS and common mode choke.

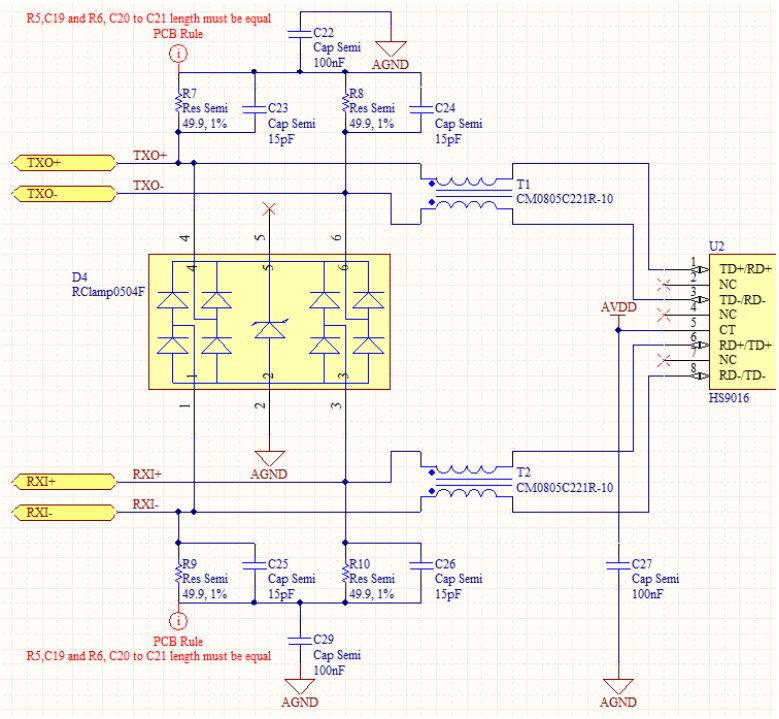


Figure 10

12. Termination resistors placement

The termination resistors should be placed as near the IC as possible after common mode choke, since each product of Davicom uses current mode to generate the voltage on the line. The fewer distance between resistor and IC, The smaller the side effect of transmission line.

13. Return current for differential pair

There are AGND pins between each pair of TX and RX. This is the end point of return current of each differential pairs. The suggestion for this kind of layout is a ground without slot through all the traces. Below, figure 11, is the illustration.

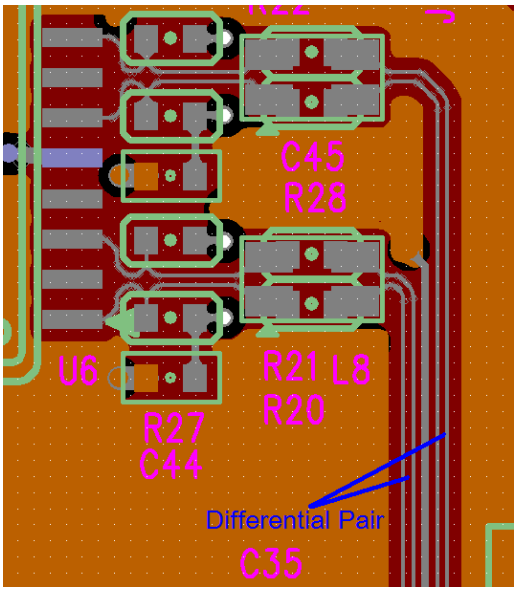


Figure 11

There are two differential pairs in thin gray. The ideal case is that there is a ground below them from transformer to IC and as what mentioned before, there is no slot line through all the pairs for maintaining the uniform of characteristic impedance and the path of return current.

14. Differential pair between transformer and connector

The differential pair here usually is placed without ground under them, in order to reduce the possibility of energy jump into the system of ESD test. The characteristic impedance is also designed to have differential impedance of 100Ω and it is almost the same to the differential lines between transformer and IC.

15. Chassis ground

Chassis ground, sometimes the same to “earth” in different design, is placed under the I/O connector for separating different ground system externally and internally.

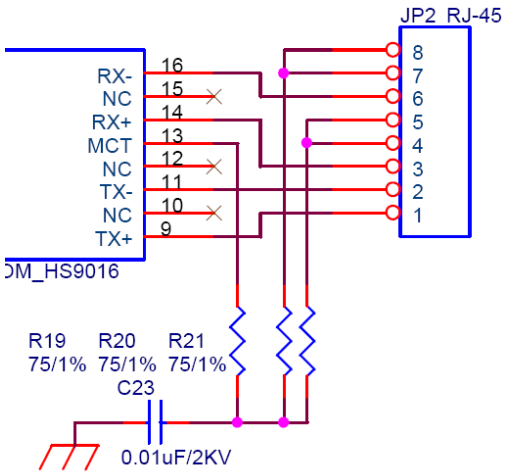


Figure 12

Figure 12 shows a connection between RJ-45 connector and transformer. There is a high voltage capacitor is used to absorb the ESD surge from cat.5e cable.

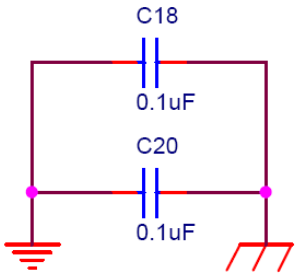


Figure 13

Two capacitors is used to link up chassis ground and system ground, like figure 13. These capacitors are normal capacitors used to lead off the ESD current to power connector.

16. TVS for PoE and ESD

TVS is a device to help the circuit immune from the incidental high voltage or current. It can be placed at any place to protect the circuit. It is usually placed on differential lines for protecting the incident wave when plug in the cable on PoE application or the ESD test.

There several kinds of TVS can be used but on differential lines, only low capacitance TVC can be used otherwise the waveform will be destroyed easily.

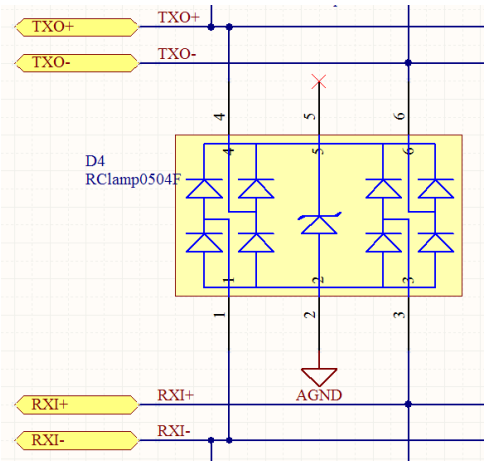


Figure 14

Figure 14 is an example schematic which uses RClamp0504F from Semtech, which is an integrated TVS with 4 clamping diode pairs and a Zener diode to protect voltage line and it has the characteristic of low capacitance (<5pF). A TVS can be placed between transformer and IC or between connector and transformer. By putting it between transformer and IC, it supports to prevent the jump in high voltage waves from other connectors which may couple to differential lines between transformer and IC. It can be placed between transformer and connector, too. It provides the protection of incident waves form the differential lines also but can't prevent the coupled waves as what mentioned before.

Modify History

Version	Modified Date	Content
1	2009/3/17	First release.
1.01	2011/5/5	Modified common mode choke.